HIGH PERFORMANCE PARALLEL PACKET CLASSIFICATION ARCHITECTURE WITH POPULAR RULE CACHING

Okanda Gamage Samoda Lakshitha

118029U

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Department of Electronic and Telecommunication Engineering

University of Moratuwa
Sri Lanka

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Abstract

As the Internet evolves novel services and applications are being introduced which require different levels of Quality of Service or non best effort service for proper functionality. Thus, there is a requirement for future networking equipment to distinguish between traffic flows belonging to different applications. The enabling function for such differentiation is multi field packet classification. Traditional software and hardware approaches to multi field Packet Classification are being challenged due to the exponential growth of internet traffic and data rates. Current growth rates of silicon technologies will not be able to handle the growth rates of Internet traffic, data rates, and rule database storage requirements in the future. Even though many research have been done in this area, packet classification technologies that support scalability in both line rates and rule sets is scarce.

We try to address these issues through a hardware architectural approach for packet classification. We identify that classifying multiple packet streams simultaneously by utilizing immense parallelism offered by modern hardware technologies while sharing a common rule database among several packet classification modules is the solution to the ever widening gap between Internet data rates and silicone speeds. Main contribution of this work is design and implementation of a packet classification architecture which has following characteristics: scalability in terms of both throughput and number of rules, capability of classifying parallel packet streams simultaneously, capability of using temporal locality of Internet traffic to increase the classification throughput by identifying classification rules which are popular among incoming packets and caching them in private caching entities in classification modules to avoid contentions at the shared rule database.

Simulation results revealed that proposed architecture is capable of achieving a throughput of more than 200Gbps for worst case packet size of 40 bytes. Proposed architecture was implemented on NetFPGA platform and the classification was done at full line rate.

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Contents

List of Figures

List of Tables

List of Abbreviations

ACL	Access Control List
ASIC	Application Specific Integrated Circuit
CAM	Content Addressable Memory
CPU	Central Processing Unit
CR	Contention Resolver
DBS	Discrete bit selection
FDDI	Fiber Distributed Data Interface
FPGA	Field Programmable Gate Array
FTP	File Transfer Protocol
HTTP	Hypertext Transfer Protocol
IP	Internet Protocol
LAN	Local Area Network
LPM	Longest Prefix Matching
PPM	Private Prefix Memory
PPP	Point to Point Protocol
PRC	Private Rule Cache
QoS	Quality of Service
SMTP	Simple Mail Transfer Protocol
SRAM	Static Random Access Memory

TCAM	Ternary Content Addressable Memory
TCP	Transmission Control Protocol
UDP	User Datagram Protocol
VoIP	Voice over Internet Protocol