

INSTRUCTION SET ARCHITECTURE DESIGN FOR VIDEO PLAYBACK DEVICE

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of Science in Electronics and Automation

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DECLARATION

I declare that this is my own work and this thesis does not incorporate without acknowledgement any material previously submitted for a Degree or Diploma in any other University or institute of higher learning and to the best of my knowledge and belief it does not contain any material previously published or written by another person except where the acknowledgement is made in the text.

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The above candidate has carried out research for the Master's thesis under my supervision.

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DEDICATION

To my family members and teachers

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ABSTRACT

Instruction Set Architecture Design for Video Playback Device

Keywords: Low Power, Processors, FFmpeg, decoders

Application specific processors are being considered for many applications which are used to run on general purpose processors. The primary reason for this is the enhanced energy efficiency while meeting the required performance targets. This thesis explores the design of Instruction Set Architecture (ISA) for a video playback device.

Video is ubiquitous today due to camera being a standard accessory in mobile phones. Video, at the same time, is a powerful learning tool for any age group particularly for younger children. The primary objective of the work is to develop a minimalist ISA for a single function video playback device which would allow longer run time on battery (enhanced energy efficiency) and low silicon footprint to minimize cost. This would allow video playback device to function without an operating system.

An extensive survey of low power processors was followed by a thorough investigation of essential assembly instructions for video playback using the industry standard video playback tool-ffmpeg. The minimal ISA developed was then validated by using Intel Software Development Emulator through dynamic run-time analysis of ffmpeg trace. Here most frequently used assembly instructions were found to be present in the minimal instruction set.

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LIST OF ABBREVIATIONS

Abbreviation	Description
TFT	Thin Film Transistor
OLPC	One Laptop Per Children
WMMX2	Wireless MMX2
LPDDR	Low Power Double Data rate memory
MIPI	Mobile Industry Processor Interface
DSI	Display Serial Interface
HSI	Horizontal Situation Indicator
SLIM	Simple Login Manager
MMC	Microsoft Management Console
HDMI	High Definition Multimedia Interface
PHY	Marvell Fast Ethernet Physical Layer
HD	High Definition
ISP	Image Signal Processor

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