SOLID STATE TRANSFORMER BASED HYBRID MICROGRID ARCHITECTURE FOR INCREASED SOLAR PV PENETRATION

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Degree of Master of Science by Research

Department of Electrical Engineering

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DECLARATION

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ABSTRACT

Increased penetration of rooftop solar PV is causing undesirable technical impacts on the distribution networks. It has been identified that several urban distribution transformers in Sri Lanka are exceeding fifty percent of the solar PV over the transformer capacity. Improving the hosting capacity of the existing distribution network has thus become a trending research topic in both local and international power systems industry. Among the identified technical impacts of high solar penetration are; voltage rise, harmonics and DC injection. The contribution of this study is focused on designing a new microgrid architecture that integrates the solid state transformer with zonal hybrid microgrids to mitigate the aforementioned issues. By utilizing the dc and ac ports of the solid-state transformer, the hybrid network can access the distribution system, which renders the coordinate management of the power and improves the power supply reliability. The designed solid state transformer controllers maintains the AC and DC feeder voltages. MATLAB/ Simulink platform was used to model and simulate the proposed network and to demonstrate how the proposed system has mitigated the power quality issues.

Key words: distributed generation, dual active bridge, grid tie inverters, high frequency transformer, hybrid microgrids, power quality, rooftop solar PV, solid state transformer, zonal microgrids

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LIST OF ABBREVIATIONS

Abbreviation	Description
DRER	Distributed renewable energy resource
CEB	Ceylon Electricity Board
HFT	High frequency transformer
MVDC	Medium voltage DC
LVDC	Low voltage DC
DESD	Distributed energy storage device
DCMG	DC microgrid
ACMG	AC microgrid
DSO	Distribution system operator
THD	Total harmonic distortion
MMC	Modular multi-level converter
MMP	Maximum power point
MPPT	Maximum power point tracking
PSM	Phase shift modulation
ESD	Energy storage devices

CHAPTER I

1. INTRODUCTION

1.1. Background

Growing popularity for roof-top solar PV as a distributed renewable energy resource (DRER) among electricity consumers have grown tremendously during the last decade. Increased electricity tariff, price reduction of solar products and services and the beneficial schemes provided by the government have made rooftop solar PV more popular than the other DRER. According to the future projections of Ceylon Electricity Board (CEB), the electrical power generation, transmission and distribution authority of Sri Lanka, solar PV capacity will continue to grow exponentially up to nearly 1500 MW by 2030 as shown in Figure 1-1 [1].

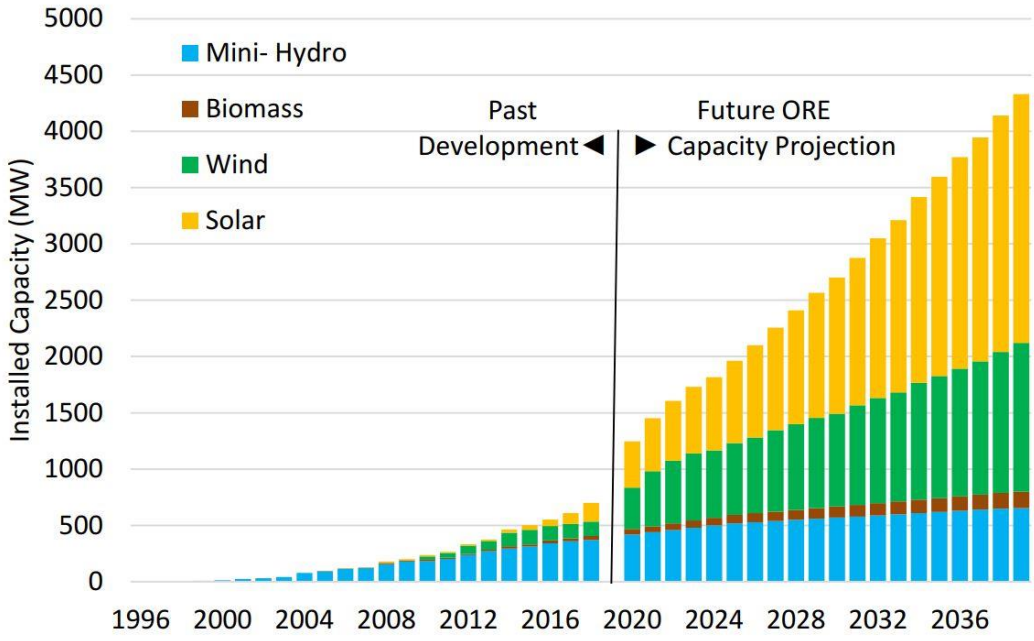


Figure 1-1: Past and future capacity development of other renewable resources [1]

However, the increasing number of unplanned solar PV connections in the distribution network could cause undesirable technical impacts on the power quality, power system reliability, and stability. Current and voltage harmonic distortion, dc injection, electromagnetic interference, voltage fluctuations, voltage unbalance and over voltage

are some power quality issues associated with the increasing solar PV installations. The solid state transformer (SST) has three power conversion stages; AC-DC stage, DC-DC isolated stage, and DC-AC stage. This is shown in Figure 1-2. The DC-DC converter consists of high frequency transformer (HFT), which provides voltage transformation and galvanic isolation. The SST features smart control capability due to its power electronics interface. The availability of DC-DC converter provides two DC buses; medium voltage DC bus (MVDC) and low voltage DC bus (LVDC) enables the direct connection of DC sources, distributed energy storage devices (DESD) and DC loads; in particularly the DC microgrid (DCMG). The presence of the AC bus at the end of the SST enables the AC microgrid (ACMG). The SST can also achieve power and energy management with improved power quality.

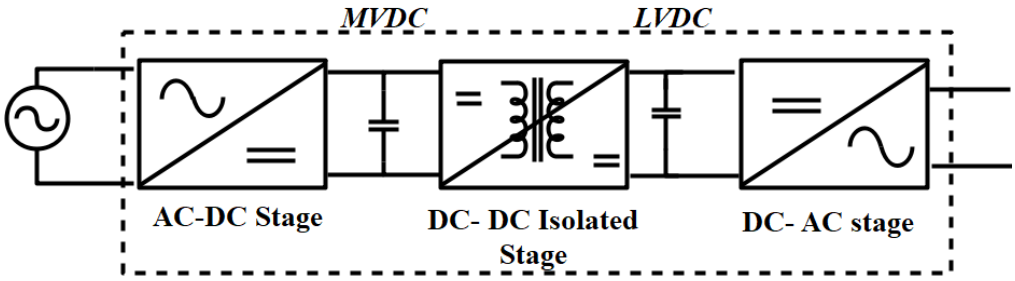


Figure 1-2: Three port SST

The SSTs are applicable in various power systems applications. Integration of SSTs with traction systems, interfacing microgrids, in replacement of the distribution transformer, as an interface to the DRER and in substations are few applications [2]. Integration of microgrids with the SST is a new trend among power electronics researchers. Microgrids facilitate increased integration of DRER and DESD to the power network.

1.2. Problem Statement

Recently, solar PV have emerged as a highly commercialized energy sector both in local and international power market. The trend of upgrading power requirements of domestic consumers through solar PV have brought economic and political benefits. However, the interconnection of the DRER into the national grid without a proper plan leads to power quality and the stability issues in the power system. Harmonic

emissions from the grid tie inverters have become significant in distribution networks [3]. In addition to harmonics, over voltage, voltage variations and flickers are the other undesirable disturbances to the distribution network caused by the solar PV.

The distribution system operator (DSO) has to maintain the power quality parameters such as voltage, total harmonic distortion (THD), total demand distortion (TDD), flicker, and DC offset under pre-defined limits. Although the existing solar PV penetration levels might not exceed the statutory limits, maintaining aforementioned limits is likely to cause significant challenges in the near future. Hence, it is necessary to investigate the power quality issues in the existing distribution network and propose solutions to mitigate the issues concerned.

However, in far future, traditional distribution networks will be converted into smart cities for enhanced liveability. Improved resilience, reliability and sustainability will be the significant factors to be considered in creating these smart cities. Community microgrids have already been established in different parts of the world supporting this concept of smart cities. In addition, clustering multiple microgrids would enhance resilience, reliability, and power quality. The proposed SST based hybrid microgrid architecture will be suitable for future smart cities with added power quality improvement and resilience.

1.3. Objectives

The main objective is to design a grid-connected SST based hybrid microgrid for increased penetration of rooftop solar PV. The specific objectives attained by the research are as follows:

I. To investigate and assess the technical issues arising from the increased penetration of rooftop solar PV using tie inverters.
II. To design a suitable model and control architecture for the SST based AC / DC hybrid microgrid in the grid-connected mode.
III. To identify how the proposed technique has supported in mitigating the technical issues arising with the unplanned interconnection of solar PV.

1.3.1. Scope

A distribution feeder with high solar PV penetration is selected from the distribution network. The feeder is modelled from MATLAB/Simulink and the power quality issues in that feeder were quantified. The scope of the study is limited to model an SST based hybrid microgrid model with a suitable architecture and controllers to mitigate the issues identified in the simulation. The developed model consists of converter stages, AC/DC loads, AC/DC sources and DESD as the requirements of the hybrid microgrid. Appropriate controllers for each converter is also designed.

1.4. Thesis overview

Chapter 1 presents an introduction to the SST based microgrid model, discussion on the problem statement and the objectives of the study are described.

Chapter 2 describes a review of previous work found in the literature on,

- Technical issues associated with increased integration of rooftop solar PV
- Why SSTs for microgrids?
- SST based microgrid architectures
- SST based microgrid control
- Experimental prototypes

Chapter 3 discusses the technical issues; particularly a power quality analysis in the existing distribution network due to high penetration of solar PV with grid tie inverters.

Chapter 4 contains the work carried out on the design of the overall system; modelling and control. This includes the zonal SSTs, AC/DC hybrid microgrids, AC/DC sources, loads and ESDs. The simulation platform employed for design and simulation in this research was MATLAB/Simulink.

Chapter 5 provides the results of the developed system which includes the power flow and power quality parameters of the system. The results are compared against the power quality parameters obtained in the existing network.

Chapter 6 discusses the conclusions of the work, the feasibility of this method to implement for real network and the future work required to improve the proposed system.

CHAPTER II

2. LITERATURE REVIEW

2.1. Technical issues related to Increased Integration of rooftop solar PV

The power quality issues of solar PV incorporates with the intermittent nature of the solar PV generation and the effects of the grid tie inverters. Table 2-1 illustrates the possible power quality issues and their causes related to solar PV [3].

Table 2-1: Power quality issues related to solar PV [3].

Category	Causes
Flicker	• Long term and short term variations due to variations in output of the generation
Slow voltage variations	• Power flow variations • Shading effects, Apparent motion of the position of the sun, change in cloud cover
Fast voltage variations	• High capacity solar PV • Tracking systems • Intermittency of the power generation due to change in cloud cover, climatic conditions • Variations in the reactive power
Over- voltage	• Solar generation (or any distributed generator (DG)) increases voltage at terminals of the generator
Voltage Unbalance	• Uneven interconnection of single phase inverters
Low order harmonics	• Harmonic network impedance affected by solar PV inverters • Primary emissions determined by the control algorithm of the inverter • Secondary harmonics caused by the background distortion and the input impedance of the inverter
Supra harmonics	• Residues from the switching in inverters • Connection, disconnection of neighbouring sources impact on primary emissions • Neighbouring harmonic sources causes secondary emissions
DC offset	• Inverters are sources of DC injection

Once a roof-top solar PV system is installed, it will be commissioned if and only if all the system parameters are within statutory limits imposed by the IEEE standards [4]. However, cumulative effects are not particularly evaluated at the commissioning level and therefore, the impact of increased integration of rooftop solar PV to the local network is found a timely necessity and has been evaluated by several research studies. Recent studies reveal that voltage levels are marginal with the existing solar PV

penetration levels in selected distribution feeders of Sri Lanka [5, 6]. The voltage THD (VTHD) levels were within the statutory limits while TDD levels were violated in many cases [6]. In these studies, the only means of harmonics injection is considered as solar PV while the effects of non-linear loads being omitted.

2.1.1. Voltage and Current Harmonic Distortion: Definitions and Requirements

$$THD = \frac{\sqrt{\sum_{h>1}^{hmax} M_h^2}}{M_1} \times 100\ \% \qquad (2.1)$$

The THD definition in equation (2.1) is obtained from IEEE 519 standard [4] where, M_h is the root mean squared (RMS) value of the h^{th} harmonic component of the quantity M, which can be either voltage or current, and M_1 is the fundamental value of the quantity M concerned. In a system-level study, TDD is more suitable to assess the impact of current harmonics at varying load conditions. It is a general practice to observe the current harmonic levels with the base as the inverter rated current, which is known as total rated distortion (TRD) [18]. However, this study employs maximum demand for the feeder at considered cases as the base to calculate the TDD. According to TDD definition given in equation (2.2), I_h is the h^{th} harmonic current and I_L is the maximum demand current at the point of common coupling (PCC).

$$TDD = \frac{\sqrt{\sum_{2}^{n} I_h^2}}{I_L} \times 100\ \% \qquad (2.2)$$

As defined in IEEE 519 standard, the recommended limits for LV VTHD and TDD are given in Table 2-2. As per the guidelines in [4], since the PV inverter falls into the power generation equipment category, the TDD limits are considered from the category $I_{sc}/I_L < 20$, hence the requirements as in Table 2-2. The I_{sc} is the maximum short circuit current at the PCC.

Table 2-2: Recommended harmonic levels [4]

VTHD	**Individual Harmonics**				
8%	5 %				
TDDD	**3 ≤ h ≥ 11**	**11 ≤ h ≥ 17**	**17 ≤ h ≥ 23**	**23 ≤ h ≥ 35**	**23 ≤ h ≥ 35**
5%	4 %	2 %	1.5 %	0.6 %	0.3 %

The DSO is responsible for providing a pure sinusoidal voltage to the customer. When the current passes through the feeder with linear series impedance there is no distortion. However, when the non-linear loads draw currents, the currents get distorted. When the harmonic currents passing through the system impedance, voltage gets distorted [7]. This is shown in Figure 2-1.

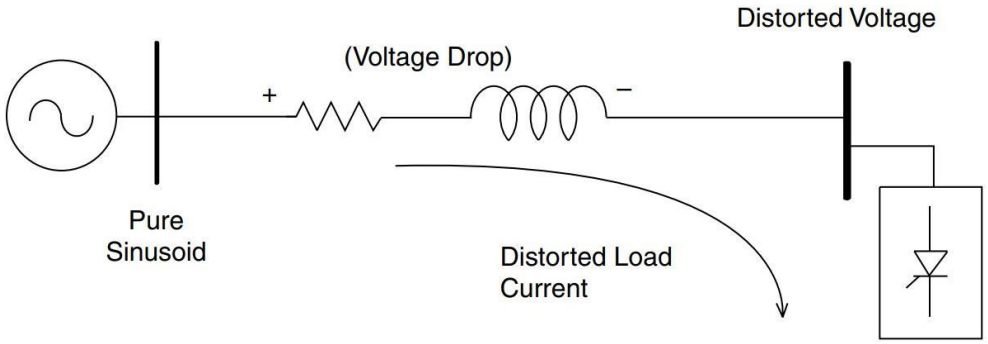


Figure 2-1: Harmonic voltages at the load caused by harmonic currents flowing through system impedance [7]

In addition to harmonic distortion, it is worthwhile to analyse the other power quality requirements related to solar PV integration.

2.1.2. Other Power Quality Parameters: Definitions and Requirements

• **Over Voltage**: The LV standards specify with a tolerance level of ± 6% of the nominal voltage to be maintained [8]. Particularly, for DG, temporary over voltage (TOV) limits are specified in [4] to be maintained at the PCC. However, this study will only consider the 6% threshold and will not focus on the TOV limits.

• **DC Injection:** According to IEEE 929-2000, the solar PV system shall not inject DC current greater than 0.5% of the rated inverter current into the utility interface under any operating condition [9]. Unlike the harmonics limits, this limit highly depends on the regulation and standards of a given country. Some countries have imposed an absolute current as the maximum limit; for an instance, Australian standards specify a limit of 5 mA as the maximum permitted DC injection where as in Germany it is 1 A [10]. The maximum allowable limit in Sri Lanka at the inverter PCC is 1% [11]. In this study, a representation of the absolute current at the system is

presented. High DC injection to the grid is harmful due to possible saturation of the transformer.

• **Voltage Unbalance:** The unbalance voltage under operating conditions for a period of 1 week of the 10-minute RMS value of the negative sequence voltage unbalance factor (VUBF) shall be 2%. A VUBF of 3% is allowed occasionally [12].

• **Flicker:** For LV distribution systems, the compatibility levels for flicker absolute short term - P_{st} and long-term flicker - P_{lt} indices are 1 and 0.8 respectively [13]. In [14], flicker measurements for 3.5 kW grid connected inverters have not displayed any violations. Assessing the flicker levels in high capacity inverters might be a potential future study since the low capacity inverter would not induce any considerable voltage variation if the grid is sufficiently stiff.

2.2. Integration of SSTs with microgrids

2.2.1. Microgrids

Microgrids with smart features have now emerged into commercial markets from laboratory setups. A microgrid is formed by integrating loads, DGs and DES. It must be able to connect and disconnect from the grid to operate in both grid-connected or island mode. To enable the seamless transition between modes, the microgrid must be of high controllability [15]. Power electronic converters are particularly employed for controlling and managing the power flow in the microgrid. The advantages served by the microgrids in the future power system are to reduce network congestion, integration of DRER, reduce network upgrades and increase the overall system efficiency and reliability [15].

The microgrid usually includes a conventional low frequency transformer (LFT) interfacing the medium voltage (MV) grid and distribution system to obtain the galvanic isolation at the PCC.

2.2.2. SST

The SST is defined as a HFT integrated with power electronics converters. For the high-frequency operation, a power electronics device is connected in series with the transformer and it provides an alternative to the LFT. Nonetheless, the SST is not a direct replacement of LFT, but has the ability to perform multiple functions. The

characteristics of the SST according to literature are: (1) voltage transformation, (2) isolation, and (3) controllability [2, 16].

The fundamental purpose of the SST is to realize voltage transformation similar to an LFT. The HFT of the SST has a lighter weight and volume compared to the LFT [2]. The increased frequencies affect the winding and core losses and ultimately there can be failures in the cooling system. Hence, the optimizing of the frequency and the size of the transformer based on core and winding material is a major apprehension, when considering the practical implementation of the SST [2]. The selection of the magnetic materials for the development of the core and the windings of the HFT are significant design considerations [2].

The 'intelligence' feature of the SST is added by its controllability. The use of power electronics makes the control of input-output currents and voltages, a possibility. In addition to the conventional features of an LFT, an SST achieves advanced power management and power quality [2, 16]. Reactive power compensation, active power flow control, power factor correction, voltage regulation and fault current detection are the other important functionalities of the SST, which can be integrated to a distribution system. Presence of the DC bus also enables the direct connection of DC sources and loads.

A general SST has three main stages: AC- DC stage, DC-DC stage and DC-AC stage as shown in Figure 1-2 (in Chapter 1). Each stage has a unique contribution in serving the aforementioned characteristics of the SST. AC-DC stage is responsible for regulating the voltage of the medium voltage DC (MVDC) link. This establishes the input of the DC–DC stage is constant and does not affect the load side voltage. The DC link in MVDC side of the DC-DC converter mitigate the voltage swell or sags from the grid; i.e. when a sag occurs, the MVDC link capacitor injects the accumulated energy and when the swell occurs, it absorbs the excess energy, so that the load voltages are not affected. Even though the on-load tap changers (OLTC) equipped for LFT can perform similar functionality in voltage regulation, a number of tap movements should be incorporated to follow variations in the voltage accurately.

As the AC-DC stage of the SST provides a constant voltage at the MVDC link, the controller of the DC- DC stage acts in maintaining a regulated DC output voltage at LVDC by allowing the required power flow facilitated by the leakage inductance of the HFT.

The AC-DC controller also provides a unity power factor and the harmonic mitigation. The rectifier stage also enables the reactive power compensation depending on the power reference enabled in the SST. The SST can isolate a short circuit fault by limiting the fault current and then trip the circuit. As an added advantage, the SST can operate in islanded mode with the SST DC- DC in isolation stage.

2.2.3. Why SSTs for microgrids

The prevailing requirements of a microgrid in future power system is listed in Table 2-3 [17]. Adoption of LFT cannot fully cover the demanding performance and functionality requirements of a microgrid [2]. Therefore, SST based microgrids have emerged as a desirable solution to accomplish these stringent performance requirements.

Table 2-3: Requirements of a microgrid [17]

Context	Requirements of a microgrid
Integration to main grid	• Isolation • Islanded operation • Transfer between operating modes
Performance	• Bi-directional power flow • Address power quality issues in distribution network • High multi-objective performance in demand side • Protection levels
Integration of sources, loads and storage	• Store and control renewable energy sources • Heavy use of DC loads such as LEDs and electric vehicles to save energy • Reduce CO_2 emissions

The existence of multiple ports in the three-stage SST is an attractive aspect for the operation of microgrids. In order to integrate the DRERs, ESDs or DC loads to the microgrid, the low voltage DC (LVDC) link can be used directly. Depending on the voltage levels, DC/DC converters are to be employed whenever necessary. With

regards to efficiency, DCMGs are more advantageous compared to ACMGs provided that the system consists of DC loads. Due to the recent developments of power electronics devices, large portion of the domestic appliances including computers, televisions, LED lightings, and sensor devices can be used as direct DC applications. Furthermore, AC loads such as refrigerators, machine drives, and induction cooking systems require variable frequency and are connected to AC through an inverter. For microgrids serving both AC and DC devices such as a hybrid microgrid, the presence of multiple ports are highly advantageous. The SST acts as a central hub to interconnect both AC and DC devices.

High penetration of DRER leads to power quality disturbances in the distribution system. These disturbances from one side of the LFT easily transfers to the other side. In terms of achieving the required power quality in a microgrid, it can be realized by mitigating harmonics and voltage sags/swells. In a fault condition, the current flow will be disturbed as the power electronic switches of the SST are turned off. The operation of SST controllers strongly affects the short circuit fault currents in the downstream network of the microgrid.

SST enabled mode and the islanding mode are the two fundamental operating modes of the microgrid. The ability of the microgrid to operate in islanding mode is determined by the available capacity of ESD connected to the SST based microgrid. The islanding mode is enabled by switching off the SST, allowing the microgrid to operate independently from the SST [18]. Bi-directional power flow is a key requirement for the interconnection of a microgrid with the main grid [19]. This grants excess generation by DRER to be fed to the grid and the bi-directionality is enabled in the SST by the DC-DC stage.

Aforementioned features can be achieved by designing the SST with a control scheme and proper architecture. Furthermore, communication schemes enabled SST improves the operational benefits of the microgrid [20]. The requirements of an envisioned microgrid system for the future distribution network are fulfilled by SSTs. At the same time, it is worthwhile to mention the design and control objectives that the SST should

fulfil to enable the interfacing with a microgrid. The design and control objectives of the SST based microgrid are:

- bus voltage regulation
- power flow control
- battery SoC management
- power quality improvement
- power factor improvement
- energy management
- fault isolation

2.2.4. Challenges on interfacing SST in a microgrid

Addressing stringent requirements of the microgrids in terms of power and energy management, improved controllability and enhanced coordination is quite challenging. Furthermore, the microgrid architecture and power electronic interfaces have significant influence in this regard. For an instance, as mentioned in [21] and [16], the DC line losses in two distinct AC/DC hybrid microgrid topologies are 24% and 56%. The variation is due to the arrangement and type of power electronic devices employed in the two topologies. Table 2-4 illustrates the summary of the identified set of challenges and proposed solutions in interfacing SSTs into microgrids.

Table 2-4: Challenges in interfacing SST in microgrids

Focus Area	Challenge	Issue	Proposed Solutions
Design	Efficiency	• Converter Loss	• Selection of the optimum switching frequency • Proper Material usage (Ex: SiC) [2]
		• Heat Transfer	• Special designs for thermal and insulation aspect [22]
	Volume/weight	• Thermal and insulation issues	• Natural convention if possible [22] • Fan-cooled and water-cooled heat-sinks [32]
	High voltage, high Power devices	• Switching ratings of power devices have to withstand the distribution level voltages (2.3 kV-35 kV) [10,22]	• Modular structures or multilevel converters [23] • Wideband gap power devices- (4H-SiC) [2]
	High frequency	• Core structure and material	• Nano – crystalline core [2]

	Transformer	• Winding configuration	• Core type solenoidal structure [2]
		• High voltage insulation conductors	• Litz wire is employed in prototypes [24]
Control and operation	Control of the SST	• Islanding mode for the isolation of the microgrid and the transfer from islanding to grid connected mode	• Presence of the DC-DC isolated stage enables the islanding mode by SST design • Different modes of operation for the seamless transfer between grid connected and islanding modes [25]
		• The complexity of the controller	• Hierarchical power management [25] • Control strategies for modular structures [37,38] • Zonal microgrid concept with SST [15] • A separate communication line for the SST coordination [17]
Cost		• Material costs • Costs incurred to improve efficiency, operating and procurement costs [16] • Short lifetime of power electronic converters [2]	• In comparison of TCO (total cost of ownership) LFT is preferred over SST [39] • Comprehensive cost analysis of the SST microgrids has not been done yet [26]
Protection	Over current	• Conventional overcurrent protection coordination incompatible with the SST [16]	• Intelligent fault detection and management [2] • External protection schemes such as solid-state circuit breakers [27]
	over voltage	• Protection of sensitive power electronic systems [16]	• LV protection; similar to the solar PV inverter • MV protection; Earthed SST high common mode stress [27] • Active protection concepts for both AC/DC SST based microgrid should be investigated further [27]
Competing approaches	Cost effective approaches for LFT	• Tap changing transformers, Distribution voltage regulators, reactive power compensators are cost effective [16]	Major selling points of SST • Fast response of SST • Full range controllability
	Hybrid Transformers	• Highly efficient (> 99%) and robust LFT with a power electronic converter for voltage control, reactive power control [4]	

2.3. SST based microgrid architectures

2.3.1. Modular Multilevel converter topologies

Because of the existing voltage and power limitations in power electronic devices and magnetic materials, for medium voltage and high power applications, the SST cells should be connected in series or parallel, in a modular structure [23]. Figure 2-2, shows a non-modular SST. Non-modular SSTs are usually employed for low voltage applications. In the microgrid application or any distribution system application, it is necessary for the SST to step down the input voltage. Hence, the LV outputs are connected in parallel and the high-voltage (HV) inputs of the SST modules are connected in series. However, these topologies use increased number of switches, resulting in added complexity and high power losses [2].

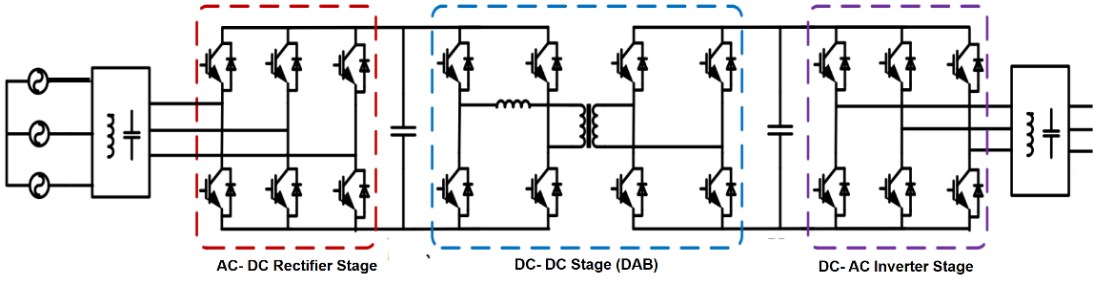


Figure 2-2: Non Modular SST Model with power switches

For the AC-DC stage, half-bridge and full-bridge configurations are applicable as a topology in one module. The full-bridge modules of AC-DC stage can be designed as a modular multi-level converter (MMC).

For the DC-DC stage, Dual Active Bridge (DAB) and the series resonant converter (SRC) can be adopted. In SRC, the switching frequency operates close to the resonant frequency eliminating the power losses, therefore providing high efficiency. However, inability of SRC to operate in multilevel voltages and to decouple the MV and LV reduce the benefits presented by the SRC. Hence, the DAB is preferred for the SST [23]. A three phase modular SST topology for microgrids, which is the generally used MMC topology is shown in Figure 2.3, [28]. Tri active bridge (TAB), quadruple active bridge (QAB), and penta active bridge (PAB) are known as multiple active bridges

(MAB) sharing a common high frequency magnetic link [29]. All these topologies are capable of providing bi-directional power flow, a required condition for the interconnection of a microgrid [23]. Having MAB with a shared HF magnetic link enhance the cross-coupling power transfer capability, better harmonics performance, and a low current stress on the LV inverter [29].

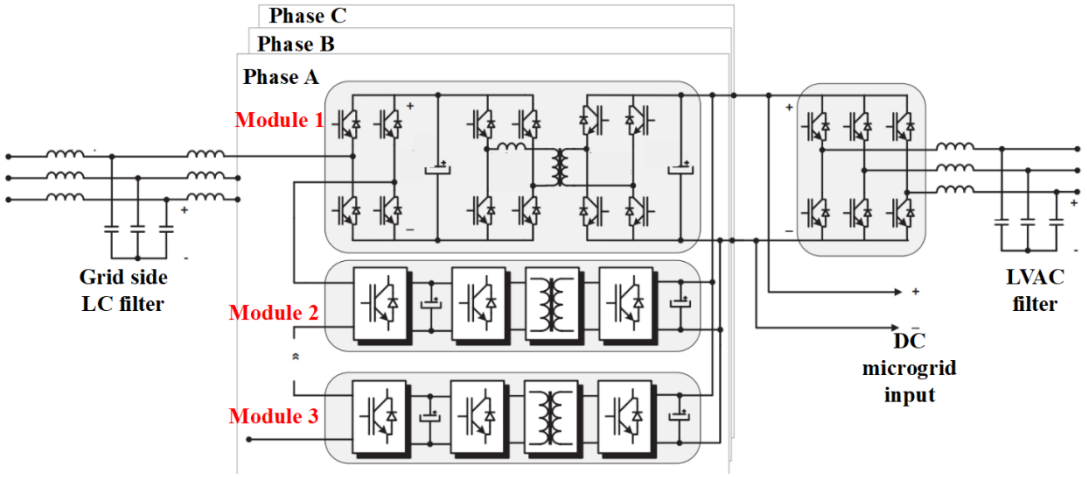


Figure 2-3: Commonly used three phase, three stage modular SST based microgrid topology [28]

For the grid applications of SST, a quantitative analysis is conducted in [30] to determine the most suitable DC-DC converter for the SST based on its efficiency. In [30], available DC-DC converter types such as the DAB, SRC, and QAB are compared. Even though its controllability is low QAB showing the highest efficiency and reliability with the low cost is selected as the best qualifier for the DC-DC stage of the SST [30]. In applying SSTs in microgrids, MMC can be adopted either in the MVAC-LVDC conversion, at the DC-DC stage or at both conversions. However, it is not essential to utilize a MMC at the inverter stage since it deals with lower voltages. Nevertheless, in some applications, MMCs are utilized at all three stages of the SST such as at the 300 kVA UNIFLEX SST [20].

A 20 kVA SST is proposed in [31] and the MMC is used at the front-end rectifier and at the DAB. Furthermore, the MMC has been adopted for both rectifier and the DC-DC conversion stage for a three phase SST in [28]. A suitable topology can be selected, depending on the voltage interface of the SST and the power handling requirement, In

[23], six types of chosen modular SST configurations based on its implementation are explained.

2.3.2. Architectures for SST based microgrids

The SST based microgrid architectures can be generally divided into two types naming microgrids with single SST and, microgrids with multiple SSTs. Figure 2.4 illustrates the classification of microgrid architectures, based on the existing and available SST microgrid configurations. Figure 2.5 further illustrates this classification. All configurations presented in Figure 2.5, presume a three stage SST topology and the DC/DC converters are not indicated wherever necessary. The microgrids with single SST, known as the "grid SST" are commonly coupled to the grid. Single SSTs are divided into two types: LVDC and LVAC connected type, and the disconnected type. The SST LVDC and LVAC disconnected type is considered as the most common and the general architecture and, it shows a few variations depending on the number of microgrids connected; i.e. Type (i) - Single microgrid with DESD, DRER and loads (Figure 2.5(a)) and Type (ii) - Zonal microgrids (Figure 2.5(b)).

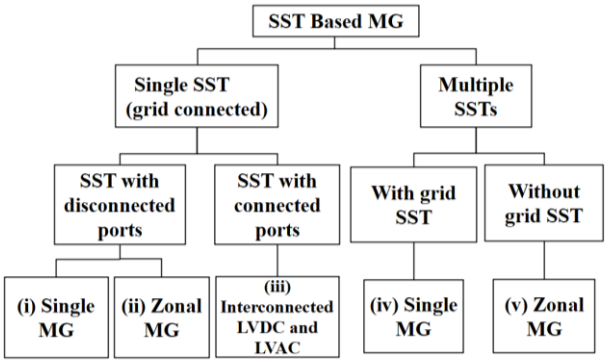


Figure 2-4: Classification of SST based microgrid architecture.

Type (i) has the simplest architecture and control scheme. It has the ability of integrating an AC, DC or hybrid microgrid. Additionally, multiple reverse conversions in an individual AC/DC hybrid microgrid are diminished [26]. The Type (ii) is a novel concept demonstrated in [18] for zonal microgrids and can be applied for a DC microgrid or AC/DC hybrid microgrid; therefore it should be reinforced with additional power management capability. However, Type (ii) shows limitations such as requirement of complex communication and control between microgrids, due to the interconnection of ports [20].

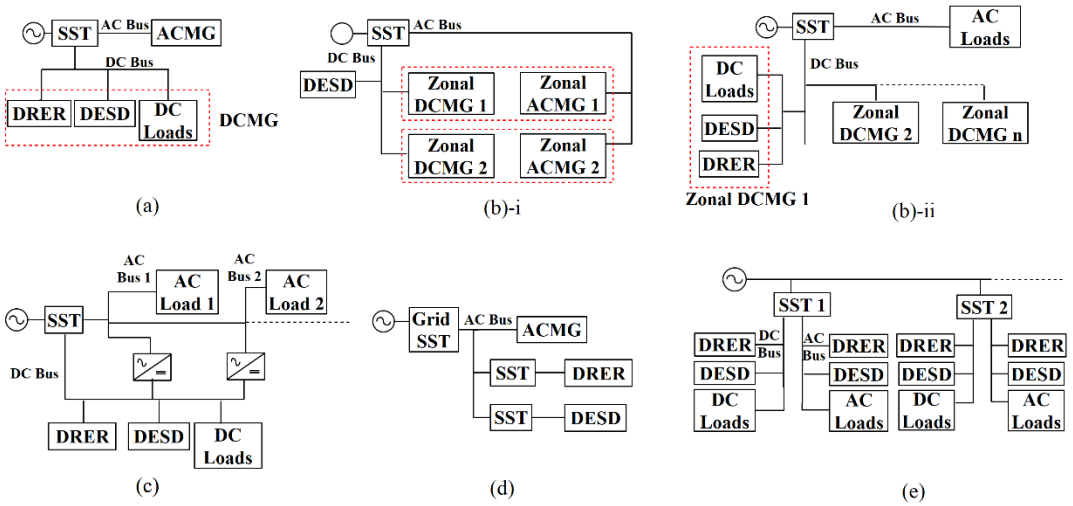


Figure 2-5: SST based microgrid architecture types (a) Type i - Single SST ,Single microgrid (b-i) Type ii - Single SST Zonal microgrids (b-ii) Zonal DCMG (c) Type iii- Single SST interconnected LVAC and LVDC microgrid (d) Type iv- Multiple SST single microgrid with grid SST (e) Type v- Multiple SST zonal microgrids wihtout grid SST

The Type (iii) - SST LVDC and LVAC interconnected concept is illustrated in [32] and is presented in Figure 2.5(c). This architecture has advantages including reduction in LV converter size, converter losses and distribution losses. As an added benefit, the voltage regulation is improved in the system due to the interconnection of the DC and AC bus. The existing microgrid architectures having multiple SSTs can be divided into two forms: as with and without grid SST. The SSTs can be directly interfaced to DRER or DESD.

As denoted in Figure 2.5(d), Type (iv) is a multiple SST architecture with a grid connected SST, which can be utilized with source and storage SSTs as well as with the ACMG. A decentralized control can be achieved with this type of architecture. In [33], same architecture is employed without the grid SST, where the SST has interfaced a wind generation. It is shown that the DG hosting capacity has improved to 60% with the use of SST. Even though the controllability is a huge challenge, many research work involve with interfacing the large-scale wind generation with SST [33]. With Type (iv) architecture, large DGs can be interfaced to the distribution network. In this event, since the SST has to operate in much lower voltages, the option of MMC

can be disregarded. The Type (v) microgrid without grid SST has an SST at each separate zone and is illustrated in Figure 2.5(e) [17]. This architecture is presented by the Future Renewable Electric Energy Delivery and Management system (FREEDM) researchers. It has complex control schemes and therefore, hierarchical strategy is proposed [26]. This architecture is convenient mainly for large regional networks.

All the above architecture types can be categorized based on energy storage as well, i.e. with a common DESD or each zone/SST having a separate DESD. For an instance, as shown in Figure 2.5(b)-i, the Type (ii) can have a central DESD with multiple Zonal microgrids and each Zonal microgrid can have an independent DESD.

2.3.3. Zonal microgrid concept

A sustainable and smart building is a promising solution that makes full utilization of DRER and ESD by utilizing power management strategies. In [18] each building or a group of buildings is regarded as a zone, within which the power is balanced. This means the buildings can supply their own power demand by using DRER and DESD. The zonal sustainable and smart building will have minimum effect to the main grid. In [18], DCMG has become the research target for the zonal microgrid concept due to the high conversion efficiency. Due to the advantages offered by AC/DC hybrid microgrid, zonal hybrid microgrids is utilized in this study. Advantages of hybrid microgrids can be listed as [34]:

- Facilitate the direct integration of both AC and DC loads/sources and DC storage with minimum conversion stages
- Minimum modification to the existing distribution network
- Efficient way to integrate the upcoming EVs (electric vehicles) units
- High reliability from grid connected mode with no backup power

The concept of zonal microgrids is employed in this study to separate domestic customers based on their region and total maximum demand in one region.

2.4. SST Based Microgrid control

The performance of SST based microgrid primarily depends on its controllers. For the reliable operation of a microgrid, it is necessary for power control scheme to operate under different modes.

2.4.1. Power flow of the SST

The most commonly utilized architecture for the DC-DC converter is the DAB, which is controlled using phase shift modulation (PSM) [19]. The direction and magnitude of the power flow of DAB can be controlled, similar to the conventional power transmission in AC power system, [35]. The inductor current i_L is changed by the phase shift of the primary and the secondary voltages of the HFT. As illustrated in Figure 2.6, the only difference between the conventional AC transmission and DAB is the power frequency and high frequency employed respectively. At high frequency, the transformer magnetizing inductance becomes negligible and the HFT can be represented by its leakage inductance as in Figure 2.6.

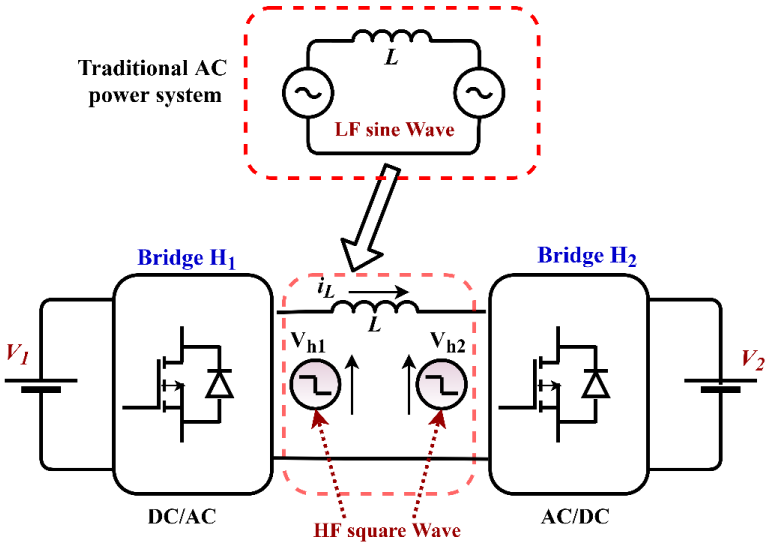


Figure 2-6: Basic power flow principle of conventional AC system Vs DAB

The power flow of the DAB is given by (2.3) where, V_{in} , V_{out} are the input, output voltages of the DAB, θ is phase angle displacement of the input voltage and output voltage of HFT (with a unity turns ratio), f is the switching frequency and L is the leakage inductance of the HFT. θ is regulated to generate the switching signal using PSM. When θ is zero, there is no power flow in the converter. When $\theta < 0$ power flow is towards the grid from the microgrid and when $\theta > 0$, power flow direction is towards the microgrid from the grid [19]. Figure 2.7 shows DAB power flow.

$$P_{out} = \frac{V_{in}V_{out}\theta}{2\pi fL}\left(1 - \frac{\theta}{\pi}\right) \qquad (2.3)$$

However, having only one degree of freedom, limits the PSM to manage only average output power. The equation (2.3) can be rewritten with the phase-shift ratio $\boldsymbol{D}$ ($D = \frac{\theta}{\pi}$), as expressed in (2.4) [35].

$$P_{out} = \frac{V_{in}V_{out}}{4fL} D(1 - D) \qquad (2.4)$$

The dual-phase-shift modulation (DPSM) with two degrees of freedom is another modulation scheme implemented for DAB and other MAB topologies. [35]. Apart from the phase shift between the primary and secondary side, it regulates the phase-shift between half-bridges in the identical sides [35]. This is presented in (3) where $\boldsymbol{D_1}$ and $\boldsymbol{D_2}$ denote the inner phase shift and the outer phase shift ratio of the DAB [35].

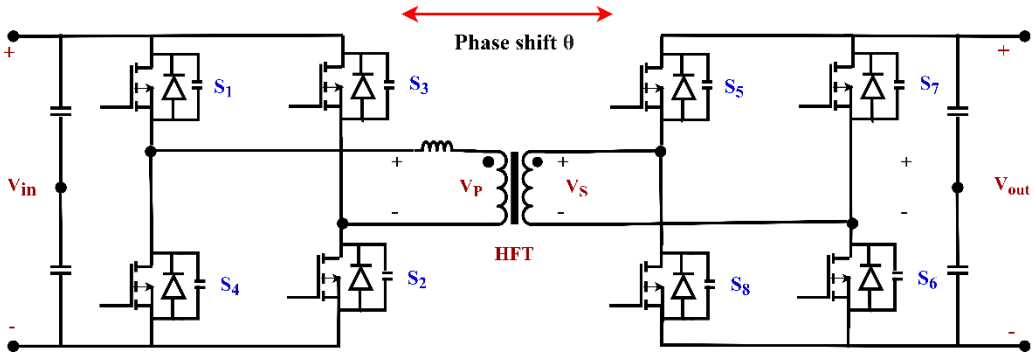


Figure 2-7: Phase shift control of SST

2.4.2. Control strategies adopted in SST based microgrid control

To maintain the power balance, the power consumed by loads of AC and DC microgrids, PLOAD should be equal to the sum of the power supplied by the SST, PSST, power supplied by the sources of the DCMG, PDC_MG and the ACMG, PAC_MG [25]. This is the main control objective of a SST based microgrid system and is shown in equation (2.5).

$$\boldsymbol{P_{SST} + P_{DC\_MG} + P_{AC\_MG} = P_{LOAD}} \qquad (2.5)$$

The SST based microgrid control strategies discussed in literature are viewed under three categories naming centralized control, decentralized control and hierarchical

control [36]. To cater the control requirements of microgrids, centralized and decentralized schemes have been the common control solution. However, more advanced controlling schemes must be employed due to the challenging control requirements imposed on microgrids. The hierarchical control for SST microgrids was presented in [25] to mitigate these challenges. A discussion on each of these strategies are presented in [37]. A comparison of each control strategy as presented in Table 2-5.

Table 2-5: Comparison of control strategies adopted in SST based microgrids.

Type	System Architecture	Control Objectives of the SST	Controllers/Techniques adopted
Centralized control	• Three stage, three phase back to back multilevel UNIFLEX System [20] • Three phase modular multilevel DC/DC converter [38] • DAB with an islanded DCMG [39]	• Universal and flexible Power Management	Predictive, deadbeat type current control technique
		• Regulate the DC output voltage • Bidirectional power flow	PWM, ZVS, dual-phase-shift method
		• Voltage regulation at the DAB at both steady state and at dynamic state	Fuzzy logic controller
Decentralized control	• Three stage, single phase SST with DCMG [19] • Three stage, three phase modular topology [40] • Three stage, single phase SST with zonal DCMG [18] • SST with cascaded multilevel rectifier and DCMG [36]	• AC-DC: MVDC Bus voltage regulation • Bi-directional power flow and maintain unity power factor at the MVAC side	PWM with dq controller for voltage and current
		• DC-DC: LVDC Bus voltage regulation	PSM
		• DC-AC: LVAC Output voltage regulation	Sinusoidal PWM with dq control
		• DC Link capacitor voltage Balancing for the rectifier • Minimize the coupling effect of the system control and voltage balance control	PI controllers for voltage balance in each H bridge
Hierarchical control	• Cascaded multilevel rectifier with three H-bridges [16] • Modular multilevel rectifier+ DAB with smart microgrid [17]	• Primary control: DC Bus voltage regulation by the battery at islanding mode	Droop control
		• Secondary control: Maintain DC Bus voltage of the microgrid	PI controller for voltage compensation
		• Tertiary control: Battery operation in the SoC range, Power, fault and energy Management of the microgrid	Upper level control structure which sets ref parameters to primary control

2.5. Experimental prototypes

This section presents, SST based microgrid test systems developed worldwide.

2.5.1. Future Renewable Electric Energy Delivery and Management System - FREEDM system

The FREEDM system is employed as a test-bed in many research presenting design and control ad techniques for SSTs [17]. The system architecture used in the FREEDM system is of Type (v) mentioned in the above section. The system compromises of multiple SSTs enabled with a fault indication device (FID) and communication. In [17], advanced cascaded control based on 4 control levels; (i) user level, (ii) SST level, (iii) FREEDM system level and (iv)multiple FREEDM system level is proposed. The control objectives at levels 1-3 are (i) demand management, (ii) DC bus voltage regulation, power management, and power quality maintenance and (iii) fault management and energy management, respectively. Level 4 control coordinates multiple FREEDM systems which form a large regional grid. A hierarchical power management strategy for the FREEDM system is depicted in [25]. The latest Generation IV SST developed by FREEDM System is 7.2 kV AC /24O V AC /400 VDC, 40 kHz SST. This system has shown an efficiency of 97.5% at 10 kW [17].

2.5.2. LEMUR project

The LEMUR Project has a 150 kW SST with a DC link (750 VDC) where a DCMG is connected, and two AC links (375 V AC, 750 V AC) where multiple nano microgrids are connected. The DCMG is connected to the interconnected LVAC and LVDC. The proposed system architecture is of Type (iii) discussed in the above section. The LEMUR project has noted an efficiency of 97.17% including the IGBT losses at 100% loading level. It uses a TAB with centralized controller for current and voltage regulation [41].

Highly Efficient and Reliable smart Transformer - HEART projectThe HEART project offers a modular approach for the ‘smart transformer’ [30]. In order to overcome the challenges of efficiency and reliability, the HEART researchers have used a modular approach. A scaled down three phase SST prototype of 100 kW, 1.5 kV 800 VAC, 800 VDC with a QAB converter is developed. It consists of three cells of cascaded half-

bridge at each phase [42]. The main control objectives of the controller are to control the local loads and sources while controlling the voltage of the MV and LV network. The developed SST in HEART project was also used for the replacement of an LFT in a distribution feeder and recorded a 60% improvement of DG hosting capacity in wind generation [42].

CHAPTER III

3. POWER QUALITY ANALYSIS: EXISTING NETWORK

3.1. Modelling the existing network

3.1.1. Modelling LV network

High solar PV penetrated distribution network which was 40% of solar PV capacity over the distribution transformer capacity (for 2018 May) of Lanka Electricity Company (LECO) is selected for the study. The network is modelled in MATLAB/Simulink, and smart meter data recorded in May 2018 were used for the model. The network consists of 3 feeders, but only one feeder was selected for the study. The details of the feeder are shown in Table 3-1.

Table 3-1: Details of the selected LV network

LV Network component	Value
Transformer	250 kVA 11 kV/400 V
Feeder location	Kotte
Maximum demand	192 kVA / 352 customers
Conductor type	ABC : 3x70 mm^2+ 54 mm^2 (R = 0.443 Ω/km , X = 0.26 mH/km)
Selected feeder	No 2 from 3 feeders /82 customers
Feeder length	400m
Maximum feeder demand	70 kVA (67 kW+ 21 kVar)
Solar customers	9 (48 kW)

The poles of the feeder were reduced using the full feeder reduction method in [43]. The feeder was reduced to 13 poles as shown in Figure 3-1. Energy consumption at each pole of the selected feeder was taken for the calculation of loads. Data was collected in every 15-minute period and the average load consumed at each pole during different times in the day was considered based on the load curve of SL. Three-time ranges in the load profile were selected based on the demand as, (i)12 am to 4 am, (ii) 10 am to 4 pm, and (iii) 6 pm to 10 pm.

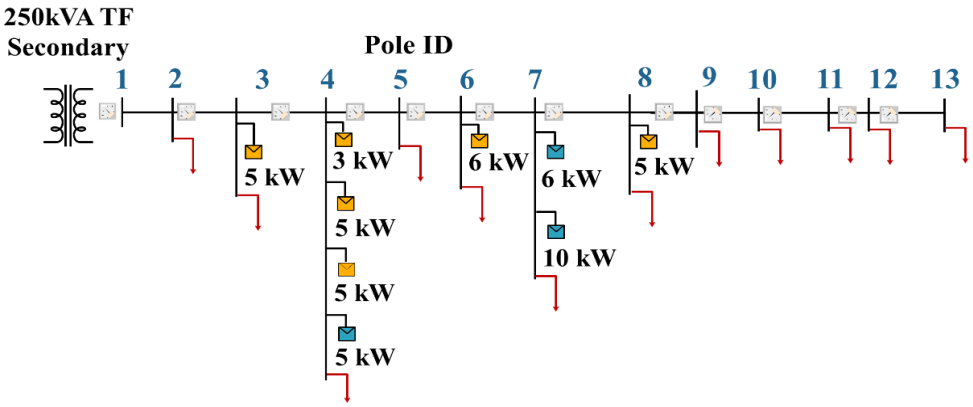


Figure 3-1: Modelled network

Two different loading levels were considered since the effect of solar penetration has to be studied. High loading was defined above 90 % of the maximum feeder loading and low loading was defined below 30 % of the maximum feeder loading during the daytime. The load variations along the feeder are shown in Figure 3-2. Different scenarios that were simulated are shown in Figure 3-3. Scenario 1 considers 100% linear loads while Scenario 2 considering 50% of the loads to be non-linear.

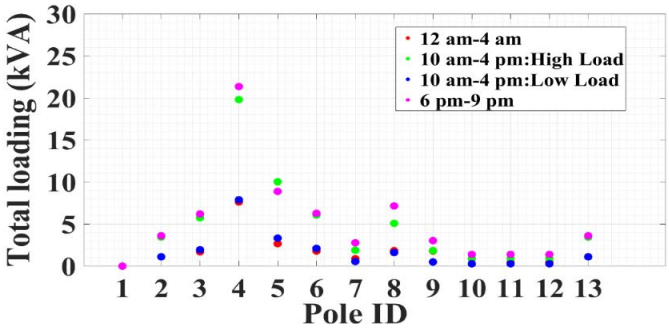


Figure 3-2: Feeder loading levels at 4 different times of the day

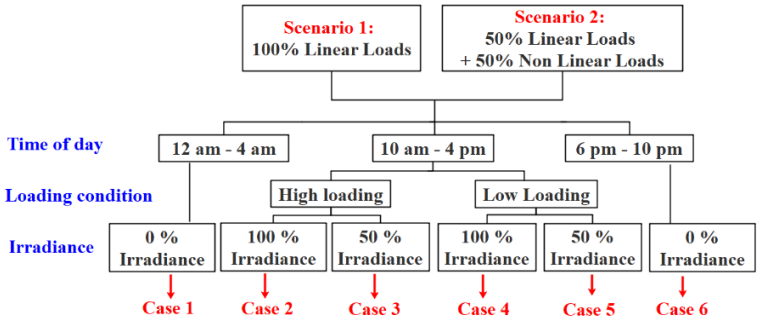


Figure 3-3: Scenarios and cases considered in this study

Non-linear loads such as computers, fluorescent lamps, induction motors with variable speed drives (VSDs) and the recent trends of usage of inverter-based motors and compressors in domestic appliances such as air conditioners, refrigerators, and the washing machines are also major concerns on the power quality of the distribution network. According to [44] around 69% of the modern domestic load may now be comprised of non-linear loads. Due to the unavailability of data for the penetration level of non-linear loads in the considered network, 50% of loads are considered to be non-linear, and modelled accordingly. The non-linear load was modelled as a resistive load is connected across a diode bridge [45] as shown in Figure 3-4.

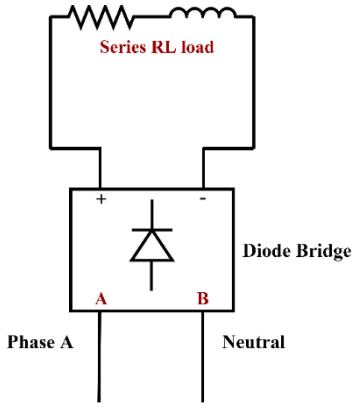


Figure 3-4: Non-linear load model

3.1.2. Modelling of solar PV System

Detailed three phase and single phase solar PV systems were developed in MATLAB/ Simulink. The complete solar PV system is discussed in this section under the following components.

I. DC components
II. Single phase/ three phase inverter
III. LC filter

3.1.2.1 DC components

For the solar PV array in SIMULINK, Yingli Solar (China) YL260p-35b was selected since it is commercially available in Sri Lanka. A study conducted on the solar assessment in Sri Lanka has shown that the maximum irradiance can reach up to 1000

Wm^{-2} [46]. Therefore, considering the hourly insolation variation, three scenarios are considered:

- 100 % irradiance at daytime (1000 Wm^{-2})
- 50 % irradiance at daytime due to shading effects (500 Wm^{-2})
- 0 % irradiance at night time

Temperature was kept constant throughout the simulation at 25 ºC. Solar PV capacities of 3 kW, 5 kW and 10 kW were employed in the model. PV array is a built-in block in SIMULINK, which is made of strings of PV modules connected in parallel. Each string consists of modules connected in series. Yingli Solar (China) contains 72 cells per module and the maximum power module is given as 260 W. To generate 5 kW power, 10 series connected modules with 2 parallel strings were employed.

Both single phase and three phase grid connected inverters were employed in the designed network considering both single phase/ three phase solar customers. In general, 3 kW panels were used only by the single phase customers, whereas three phase customers use 5 kW or above. For the solar PV and the inverter connection the necessity of a DC-DC boost converter depends on the output voltage generated by the solar panel. For single phase, the minimum voltage at the solar PV side is 325 V (230 $\times\sqrt{2}$) and for 3 phase, it is 565 V (400 $\times\sqrt{2}$). According to [47], even at a sunny day, at maximum power generation, maximum temperature in Sri Lanka is identified to stay below 60 ºC. The PV characteristics at different temperatures for Yingli solar PV array 3kW and 5 kW is shown in Figure 3-5(a) and (b) respectively. For 3 kW, the maximum power point (MPP) array voltage of the solar PV does not reach below 325 V even at the maximum temperature [47]. Hence a boost converter was not used for 3 kW single phase inverter. However, a boost converter was used for the 5 kW and above three phase inverters.

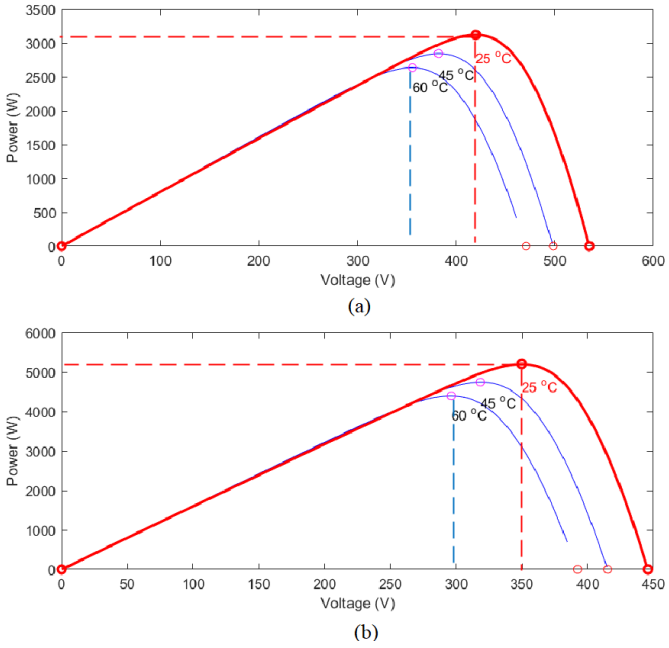


Figure 3-5 MPPT characteristics at different temperatures of PV array(a) 3 kW PV (b) 5 kW PV array

In order to facilitate, PV voltage variations, it is necessary to find out the PV voltage limits. From Figure 3-5 (a), the lower limit of the solar PV voltage is found as 300 V. In order to obtain the upper limit of the voltage, PV characteristics at different irradiances were used. As shown in Figure 3-6, the upper limit of the operating voltage was considered as 350 V. Hence, the boost converter has to boost the voltage from 300 VDC (V_{MPP_LOWER}) - 350 VDC (V_{MPP_UPPER}) to 700 VDC. A 700 VDV was selected as the upper limit because the three phase commercial inverter designs have employed 600 VDC- 800 VDC [48]. The design parameters of the boost converter were calculated according to [49]. Main parameters of the boost converter included;

- Switch: IGBT/Diode
- DC filter input capacitance: 1500 µF
- DC boost inductance: 4 mH
- DC capacitance: 3000 µF

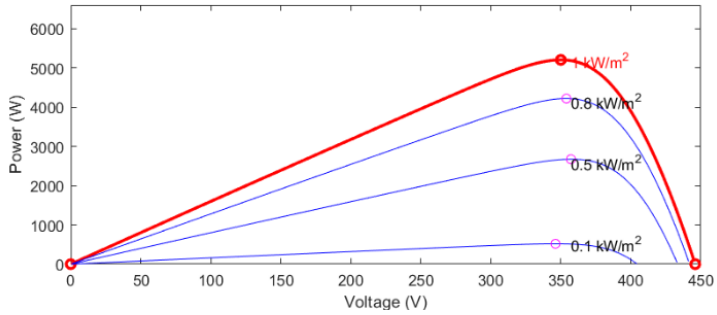
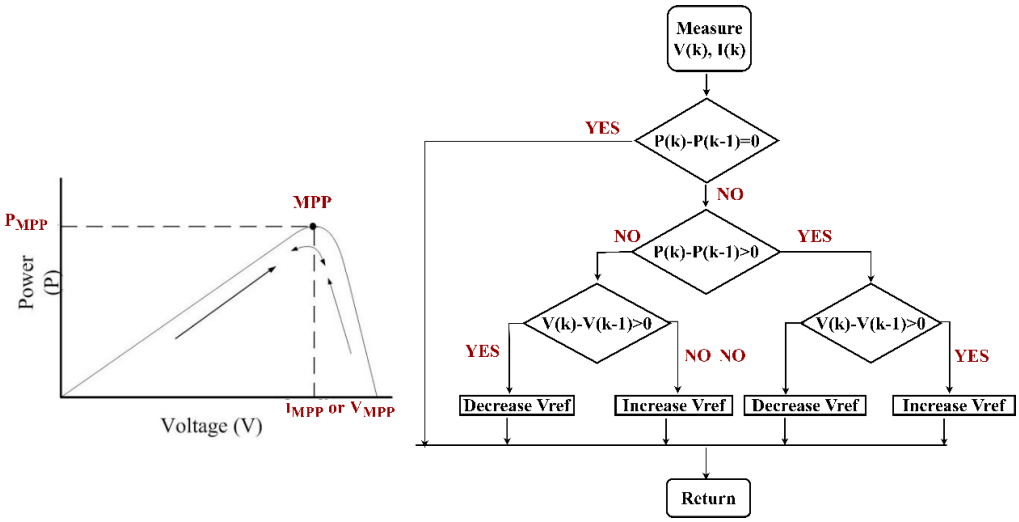


Figure 3-6:MPPT characteristics at different irradiances oW PV at irradiances of 5 kW PV array

The boost converter is embedded with a Perturb and Observe (P&O) based MPPT controller. The P&O algorithm was used due to its simplicity when compared to other MPPT algorithms. The power output of the solar panel has to be calculated after measuring the voltage, ***V*** and current, ***I*** outputs of the solar panel. The measured output power at the current instant (P_k) with the generated power at the last instant (P_{k-1}), the voltage is either increased or decreased until the maximum power point (MPP) is reached as shown in Figure 3-7 (a). This is done by increasing and decreasing the duty ratio of the boost converter (See Figure 3-7 (b)). The MATLAB code employed to implement the P & O algorithm is given in Appendix A.



(a) (b)

Figure 3-7: The P&O algorithm (a) Tracking of the MPP (b) flowchart

3.1.2.2. Single phase/ Three phase inverter

The three-phase inverter is utilized for the DC – AC voltage conversion. The Phase Lock Loop (PLL) module is used to maintain the synchronisation with the grid and to control the PWM input for the inverter. Six IGBT switches were used in three arms for the universal bridge. Since the inverter control objective should be to obtain the maximum power from the PV generation, PQ controller is used.

Let the output phase voltage of the grid tie inverter be ***v*** and peak voltage be $\boldsymbol{V_m}$.

$$\begin{bmatrix} va \\ vb \\ vc \end{bmatrix} = \begin{bmatrix} Vm\cos(\omega t) \\ Vm\cos(\omega t - 2\Pi/3) \\ Vm\cos(\omega t + 2\Pi/3) \end{bmatrix} \qquad (3.1)$$

The dq transformation is a space vector transformation of three-phase time-domain signals from a stationary phase coordinate system (abc) to a rotating coordinate system (dq0) [50]. Conversion of abc → dq yields,

$$\begin{bmatrix} vd \\ vq \\ v0 \end{bmatrix} = \frac{2}{3}\begin{bmatrix} \cos(\omega t) & \cos(\omega t - 2\Pi/3) & \cos(\omega t + 2\Pi/3) \\ -\sin(\omega t) & -\sin(\omega t - 2\Pi/3) & -\sin(\omega t + 2\Pi/3) \\ \frac{1}{2} & \frac{1}{2} & \frac{1}{2} \end{bmatrix}\begin{bmatrix} va \\ vb \\ vc \end{bmatrix} \qquad (3.2)$$

Where $\boldsymbol{\omega t}$ is the angle between rotating coordinate and the fixed coordinate. The ***0*** component above is same as the zero sequence component in the symmetrical component [50]. Further,

$$\cos(\omega t) + \cos\left(\omega t - \frac{2\Pi}{3}\right) + \cos\left(\omega t + \frac{2\Pi}{3}\right) = 0 \qquad (3.3)$$

Hence, assuming a balanced system, the ***0*** component can be opted out. Solving (3.1), (3.2) and (3.3), ***vd*** and ***vq*** can be obtained.

$$\begin{bmatrix} vd \\ vq \end{bmatrix} = \begin{bmatrix} Vm \\ 0 \end{bmatrix} \qquad (3.4)$$

Let ***i*** be the output current of the inverter. The d-axis and q-axis components of the current can also be transformed by d-q transformation. The current, ***i*** can be decoupled into active and reactive power components $\boldsymbol{i_d}$ and $\boldsymbol{i_q}$ respectively. These currents can be controlled based on the reference currents in order to control the active and reactive power. The instant AC output current is measured and converted into ***id*** and ***iq***

components and compared against the reference i_{d_ref} and i_{q_ref}. In creating the reference current time varying quantities cannot be used, hence the i_d and i_q components become useful. Since V_q = 0;

$$i_{d\_ref} = \frac{P_{ref}}{V_d} \qquad (3.5)$$

$$i_{q\_ref} = \frac{Q_{ref}}{V_q} \qquad (3.6)$$

The PLL was utilized to track the grid voltage phase angle. MATLAB PLL block can track both phase angle and frequency. In the developed inverter, only the phase was tracked since the frequency is constant. PLL block is a closed loop control system, which locks the output signal to the input signal when they are matched. It consists of a frequency oscillator, phase detector and a feedback loop. The internal frequency oscillator generates a periodic signal, which is compared to the input voltage phase. The PID controller adjusts the oscillator frequency such that the phase difference is zero. To remove the error noise, a low pass filter is used. This is shown in Figure 3-8.

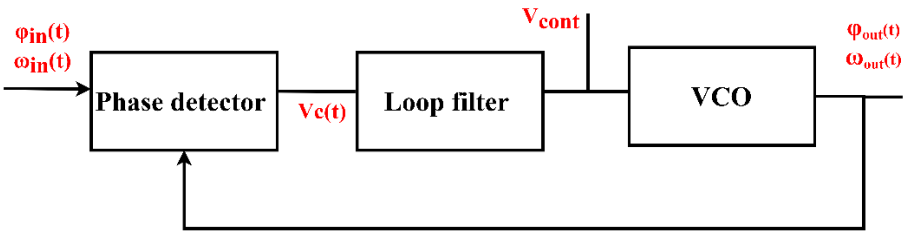


Figure 3-8: Internal diagram of the PLL controller

A PQ controller with sinusoidal PWM (SPWM) was designed. Currently, the best and the most used inverter applications employ sinusoidal PWM inverter. It produces high quality sinusoids with significantly lower THD [51]. Further, the switching pulses for the inverter are generated using the unipolar SPWM. Unipolar PWM is utilized as it results in better output power quality compared to the bipolar PWM technique [52].

The solar PV active power output and the DC bus voltage were taken as inputs to the PQ controller. With these two inputs, the d axis reference current is calculated with equation (3.5) (Reactive power is not controlled). This d axis reference current is

converted to abc frame and compared against the actual current supplied by the inverter. Gate signals are generated so as to make actual supplied current within the reference current.

To stabilize DC bus voltage, the measured voltage of the DC bus is compared with the reference DC bus voltage (700 V). Error is passed to PI controller. Output of PI controller corresponds to the power that should be drawn from grid to maintain constant DC bus voltage. Difference of PV power and this power is supplied to grid. This is shown in Figure 3-9.

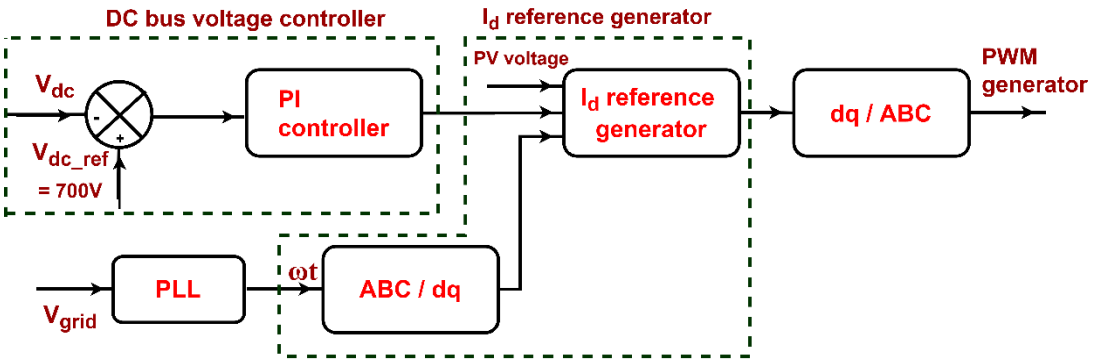


Figure 3-9: PQ controller

The single phase inverter was modelled as given in [47]. The summary of two types of inverters are given in Table 3-2.

Table 3-2: Single phase Vs three phase inverter modelling

Single phase inverter	Three phase inverter
Single phase full bridge IGBT/ Diode	3 phase universal bridge with IGBT/ Diode
No boost converter	DC boost converter (350- 700 VDC)
2 level Unipolar PWM generator	2 level Unipolar PWM generator
MPPT Tracking – Perturb and observe algorithm	MPPT Tracking – Perturb and observe algorithm
PQ controller with single phase ***dq*** current control	PQ controller with three phase ***dq*** current control + 700 VDC bus voltage control

3.1.2.3 LCL filter

Harmonic filters are series or parallel resonant circuits designed to reduce or divert the harmonic currents through low impedance paths. The grid connected filter is used to filter the PWM signal from the inverter output and improve power quality of the inverter power output. Three types of filters are discussed in literature and are summarized in Table 3-3. At low frequencies, LCL and L filters have similar attenuation behavior. The LC and LCL filters both present a large resonance peak after the resonant frequency, which can cause instability to the system while L filter offers better attenuation. For higher frequencies, LCL filter has better attenuation than L and LC filter. LCL filter seems the best option when considering cost, weight and harmonic attenuation. However, the resonance peak can be eliminated by a damping resistor. LCL filters are used in grid-connected inverters and PWM rectifiers [53].

Table 3-3: Comparison of filter types

Features	**First order filter (L filter)**	**Second order filter (LC filter)**	**Third order filter (LCL filter)**
Harmonic attenuation	-20 db/decade	-40 db/decade	-60 db/decade
Resonance peak	-	Large peak	Large peak

LCL filter as shown in Figure 3-10 was designed based on the steps suggested in [53]. The L1, L2, C and R are the circuit parameters to be determined. The data employed to calculate these parameters are given in Table 3-4.

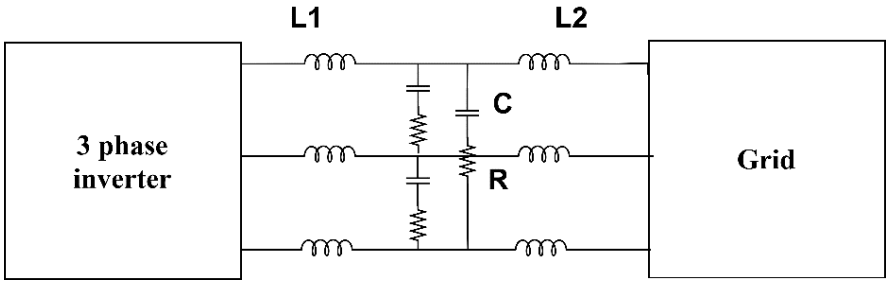


Figure 3-10: LCL filter designed

Table 3-4: Input inverter data to calculate the filter parameters

Parameter	Value
Grid frequency (fg)	50 Hz
PWM career frequency (fsw)	20 kHz
Nominal inverter power (Pn)	5 kW
Grid phase voltage (Vg)	230 V
DC Bus voltage (Vdc)	700 VDC

To calculate L1, allowed a 10% ripple current from the maximum inverter current output. From (3.7)- (3.9), ***L1*** can be calculated which yields 5.69 mH.

$$\Delta I_{LMAX} = 0.1 \times I_{MAX} \qquad (3.7)$$

Where,

$$I_{MAX} = \frac{\sqrt{2}\, P_n}{3\, V_{ph}} \qquad (3.8)$$

And,

$$L_1 = \frac{V_{dc}}{6\, f_{sw} \Delta I_{LMAX}} \qquad (3.9)$$

To calculate **C**, define the base impedance and base capacitance from (3.10) and (3.11). Let the maximum power factor variation be 5% according to (3.11). Considering a delta configuration of capacitors, the maximum capacitor value is selected as 31 μF. This was considering the capacitance to be within the limit of 5% of the base value. Rounding off to the closest commercial value, 31/3 μF for the delta connection yields 10 μF for the ***C1***.

$$Z_b = \frac{V^2}{P_n} \qquad (3.10)$$

$$C_b = \frac{1}{\omega_g Z_b} \qquad (3.11)$$

$$C_f = 0.05\, C_b \qquad (3.12)$$

The LCL filter is expected to reduce the expected current ripple value to 2% of the output current. The grid side inductor ***L2***, was designed based on the attenuation requirement. Initially, the inverter is considered as a current source at each harmonic frequency, and the LCL filter circuit was analysed. Considering the harmonic current injected at the grid, by the inverter output current,

$$L_2 = \frac{\sqrt{\frac{1}{k_a^2}+1}}{C_f \times \omega_{sw}^2} \qquad (3.13)$$

Where the desired attenuation, k_a is 2%, which yields ***L2*** as 0.0379 mH. The LCL filter has a resonance peak. Hence, to attenuate this resonance, a series resistor was used with the capacitor. The value of this resistor should be one third of the impedance of the capacitor at the resonant frequency [54]. The resistor in series with the filter capacitance is given by equation (3.13). The impedance of the LCL filter equivalent circuit is analysed to get the resonance frequency as in (3.14). The damping resistor is calculated as 1.95 **Ω** for the delta connection. The filter parameters are summarized in Table 3-5. The complete solar PV system, which consist of DC components, inverter and the LCL filter is shown in Figure 3-11.

$$R = \frac{1}{3\omega_{res}C} \qquad (3.14)$$

$$\omega_{res} = \sqrt{\frac{L_1 + L_2}{L_1 L_2 C_f}} \qquad (3.15)$$

Table 3-5: Filter parameters

Parameter	**Value**
L1	5.69 mH
L2	0.0379 mH
C	10 µF
R	1.95 **Ω**

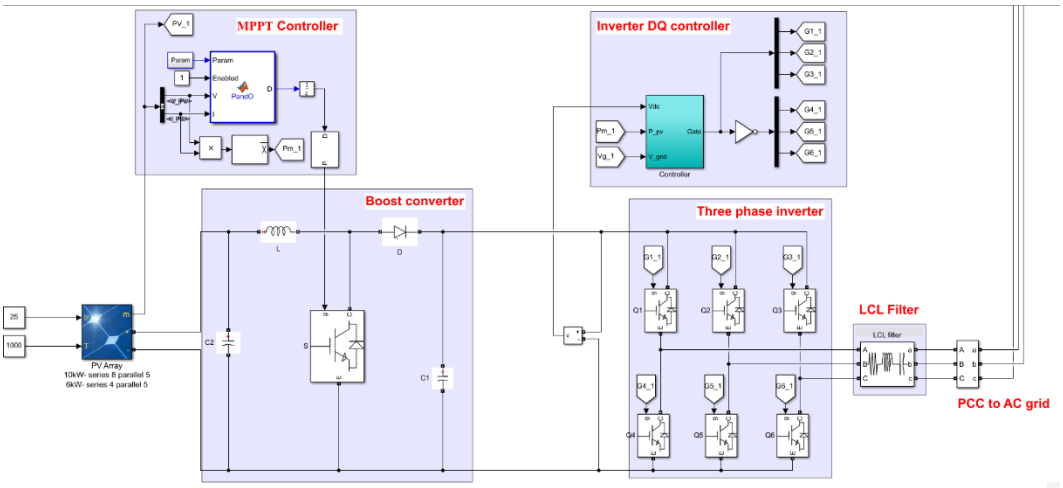


Figure 3-11: Complete solar PV system

3.2. Power Quality Measurements of Existing network

3.2.1. Types of measurements

As mentioned in Section 2.1, the harmonics and voltage rise are considered as the most common power quality issues due to high penetration of solar PV. In order to measure the voltages of the PCC at 13 poles MATLAB voltmeters were employed.

$$TDD = \frac{THD \times I_1}{I_L} \qquad (3.16)$$

The fast Fourier transform (FFT) analyser in MATLAB was adopted to calculate the harmonic. The THD, DC offset and the fundamental components were directly acquired from the FFT analyser. For the TDD calculation (See Equation (3.16)), the THD value and fundamental current component, $\boldsymbol{I_1}$ can be obtained directly from the FFT analyser in MATLAB. Refer Appendix B for further details. At each simulation case considered, peak demand current, $\boldsymbol{I_L}$ was considered as the peak current measured for over 30 minutes. Since the single phase loads and the single phase solar PV generation located in random phases of each pole replicating the unplanned connections adds a voltage unbalance to the system, the maximum demand current at any given phase was considered. The maximum demand currents for the Cases 01-06 are 31 A, 86 A, 86 A, 28 A, 28 A and 96 A respectively.

As the first step, the THD and TDD levels at the metering PCC of each inverter were measured and noticed that the levels were within the appropriate levels [4]. However, the scope of this study is to analyse the system-level impacts. Therefore, when each inverter is operated alone, the THD and TDD levels at the corresponding pole were measured and presented in Table 3-6.

Table 3-6: Power quality measurements when each inverter is operated alone

Pole ID	**3**	**4**			**6**	**7**		**8**
kW	5	3	5	5	6	6	10	5
Config.	1ph	1ph	1ph	3ph	1ph	3ph	3ph	1ph
VTHD %	0	0.09	0	0.39	0	0.39	0.33	0.06
TDD%	0.01	0.07	0.01	0.13	0.01	0.13	0.82	0.46
DC (%)	9e-4	0.053	0.003	0.04	0.002	0.04	0.06	0.04

According to the Table 3-6, the highest harmonic distortion levels were observed at the three phase inverters. The three phase inverters do not generate triplen harmonics under balance loading [7]. Therefore, rise of THD levels of single phase inverters compared to the three phase inverters is expected generally. However, due to the three-phase unbalanced loads, the effect of triplens will be significant. It can also be noted that the 3 kW single phase inverter has significant distortion levels compared to 5 kW single phase inverters.

There is an inverse relation between the power rating of an inverter and distortion level where lower the power rating of an inverter, higher distortion level is induced to the power system [55]. When system-level impact of individual inverters is considered, they present VTHD variation of 0% - 0.39% and ITHD variation of 0.01% - 0.82% and the DC offset ranges from 0% - 0.06%. When the cumulative effect is considered, with the presence of multiple harmonic generation sources, the resultant harmonic levels might either attenuate or advance [7].

3.2.2. Voltage variation along the feeder

In order to investigate the voltage variation along the feeder, the transformer secondary voltage was set to 235 V according to the collected measurement data. According to

the Figure 3-12, under the existing conditions, no voltage violation is recognized in this selected feeder having 40% solar PV generation.

Figure 3-12(a) shows voltage variation along the Feeder under Scenario 1(with 100% linear loads). Scenario 2(with 50% linear loads and 50% non linear loads) is presented in Figure 3-12(b). A similar variation is noticeable under both scenarios.

As shown in Figure 3-12(a) and (b), when there is solar power generation, a voltage rise can be seen at the poles having solar PV connected lines. This accommodates with the observations in [3], and is recognizable, when comparing Cases 01 and 06 (no solar generation) with Cases 02 – 05 (having the solar generation). Typical voltage drop along the line due to the conductor impedance can be observed in Cases 01 and 06. In the Cases 02 – 05, specially under high solar generation, voltage rise is observable up to pole 8, where the solar PV connection terminates. Then, the voltage drops along the line due to the line losses. A higher increase in voltage compared to the other cases is observable in Case 04, where there is maximum solar irradiance with low load demand. If the PV generation exceeds, in feeder loads as can be observed in Case 04, power flows back from feeder to the upstream network, which causes the voltage rise. In this case maximum of 4 V voltage rise is observed at pole 8.

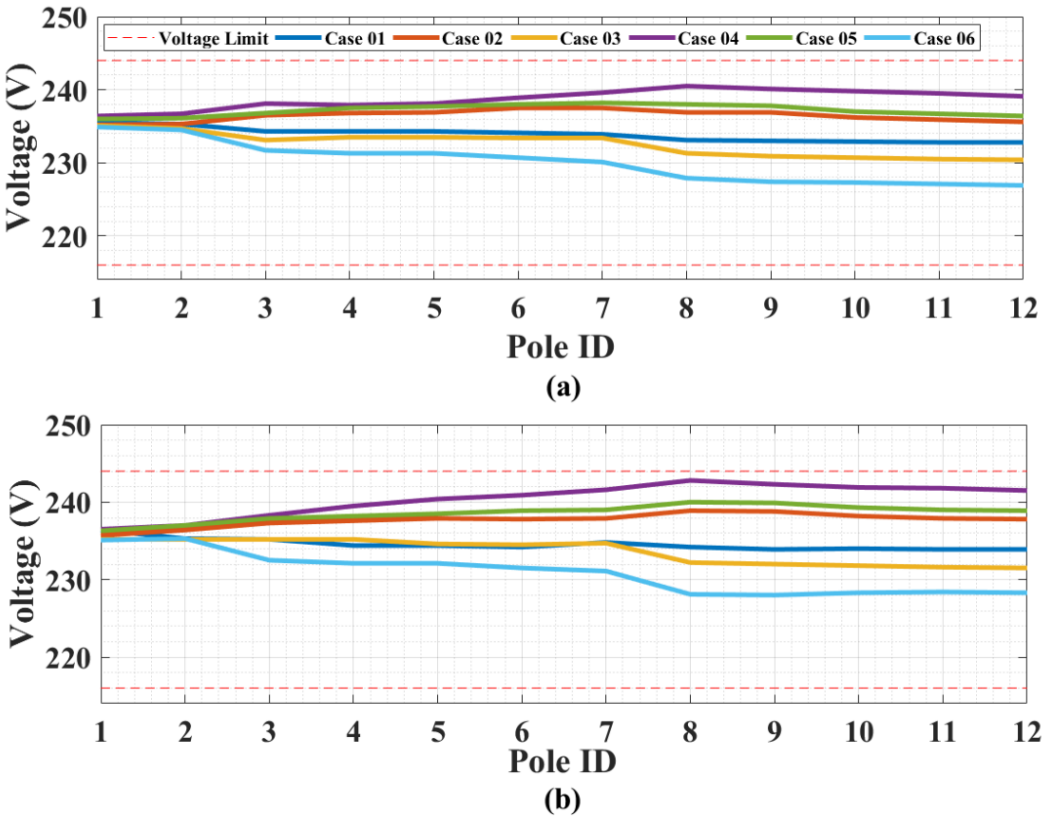


Figure 3-12:Voltage variation along the Feeder (a) Scenario 1, (b) Scenario 2

3.2.3. Voltage THD

According to the Table 2-2, it is observed that the total harmonic level; VTHD does not exceed the limit of 8%. However, individual harmonic levels might exceed the limits, but were not analyzed in this study.

A considerable voltage distortion is expected, when the individual inverter operation is compared against all the inverters in operation and analysing the impact of multiple inverters on system power quality is a complex and thorough study as, many factors are to be considered including, inverter control, location of the inverter and the strength of the grid. Even though a cumulative effect is expected, in some instances the harmonics can also be attenuated due to the secondary emissions. For low order harmonics, the multiple inverters might increase the harmonic levels if the grid is weak [56]. Having all the solar inverters being connected, the VTHD along the Feeder under Scenario 1 and Scenario 2 (in Figure 3-3) are presented in Figure 3-13 (a) and (b) respectively. The VTHD levels have increased considerably, when non-linear loads in

the system are taken into account. Since clean undistorted voltage waveform supplied at the transformer by the utility is unlikely to get distorted at its LV side, under both scenarios, the voltage distortion at the end of the feeder is comparatively higher than the transformer LV side.

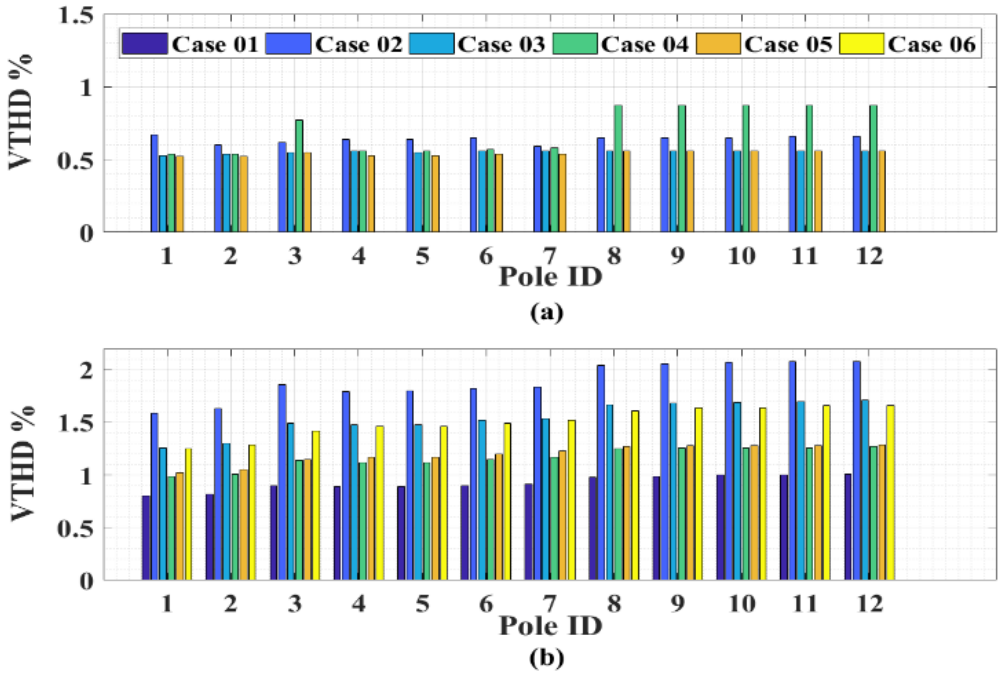


Figure 3-13: VTHD along the Feeder (a) Scenario 1, (b) Scenario 2

In Scenario 1, maximum recorded THD is 0.9 % and in the Cases 01 and 06, the THD is zero because of the absence of solar PV generation. The variation of THD incorporating the impact of solar irradiance level on the THD can be shown in Figure 3-13 (a). At all the poles, given a 50% increase of irradiance, the THD has a modest increase of around 0.1 - 0.5%. This is justified by the research done in [57], that states 1.5% - 2.2% change of THD for instantaneous fluctuations of irradiance. However, this analysis only has focused on a step change of irradiance and the THD is considered only at the steady state in accordance with the definition of THD [7]. The rise of VTHD at the feeder end is significant in low loading conditions with high PV generation (Case 04) under Scenario 1 (case with 100% linear loads).

According to the Figure 3-13(b), under Scenario 2 (case with 50% non-linear loads), VTHD levels have considerably increased in high loading conditions with high PV

generation (Case 02). However, due to the effects of non-linear loads the results do not reveal a clear relation between the VTHD and the loading condition and PV generation under Scenario 2.

3.2.4. TDD

The variation of TDD under scenario 1 and 2 along the feeder are shown in the Figure 3-14 (a) and (b) respectively. Unlike in voltage variation and VTHD levels, TDD in both scenarios is negligible or marginal to the end of the feeder from the Pole 6, but TDD limits are violated up to the pole 5 from the transformer [3]. This is in the agreement with the general tendency of harmonic current flow, which is from harmonic source towards the transformer [2]. As in Figure 3-14(a), under scenario 1, at pole 3, TDD is observed to be 18.8%. The higher solar penetration at pole 4 has increased the TDD at the pole 3.

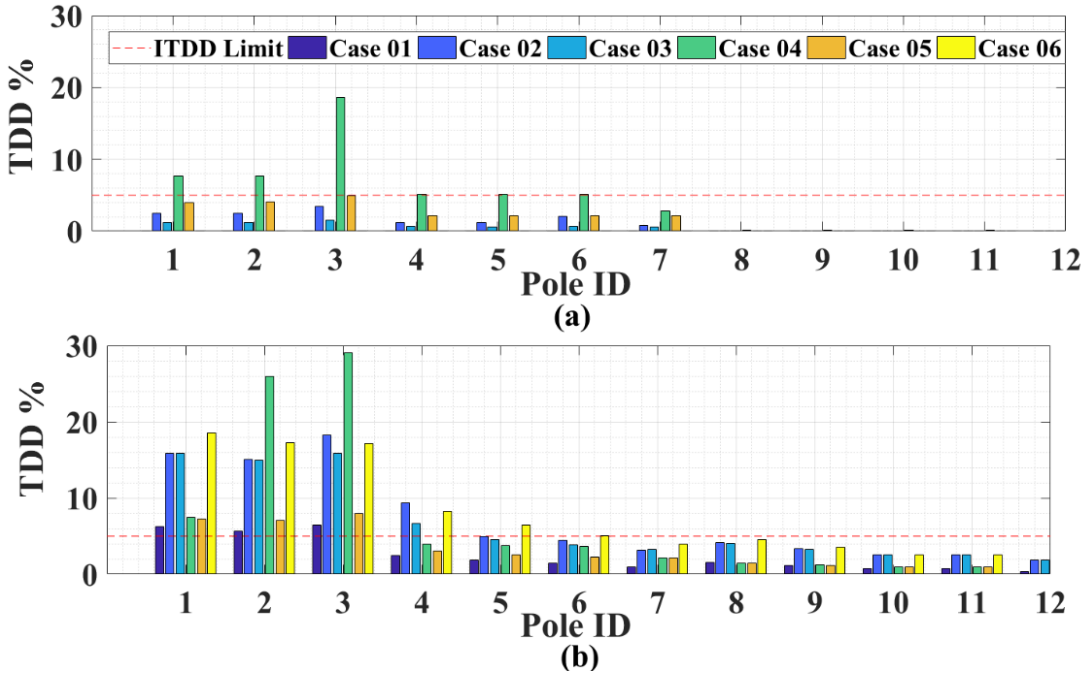


Figure 3-14: TDD along the Feeder (a) Scenario 1, (b) Scenario 2

Although it is expected the high irradiance to lower the current harmonics [36], it is not observed in this research. The two irradiance variation levels (50% and 100%) considered are not sufficient to illustrate this fact. In [36] a clear ITHD variation can be observed when the irradiance levels are changed from 10% - 50%. In Scenario 2,

in the night peak (Case 06) higher current distortion is observed illustrating the distortion levels by the non-linear loads. In the transformer end it is high as 19% and at the feeder-end it is around 3%, which is still higher compared to the other cases. As shown in Figure 3-14(b), the harmonic current towards the transformer LV side can be precisely observed in the Scenario 2. In order to acquire a finer depiction of harmonic propagation, Individual harmonic evaluation must be conducted.

3.2.5. DC Injection

The analysis of DC current injection is significant because of the following facts [7, 26]: (i) the flow of harmonic currents is towards the transformer, and (ii) Transformer core saturation due to DC current. It can be stated that, the acceptable limit of DC current injection is 0.5% at the PCC of the inverter [58]. But, in this research, the absolute DC offset at the poles are presented.

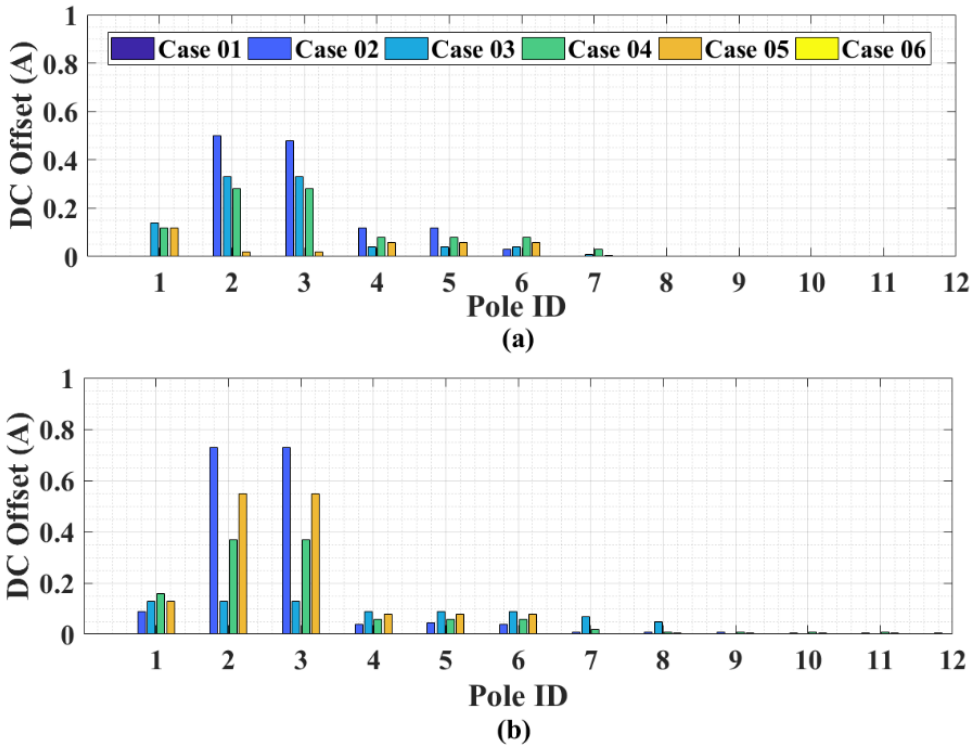


Figure 3-15: DC Injection along the Feeder (a) Scenario 1, (b) Scenario 2

The DC injection along the feeder under Scenarios 1 and 2 are shown in Figure 3-15 (a) and (b) respectively. According to the Figure 3-15 (a), a DC offset of more than 0.1 A is observed upto pole 7, which is remarkably undesirable. For an instance, at the

inverter PCC (5 kW, 1 phase) a 0.5 A of DC offset will produce a DC injection of 2.3%. It can be said that the rise of DC offset depends on the high solar irradiance regardless of the load non-linearity. At the feeder end, the DC current is low because of the absence of solar PV at the end of feeder.

CHAPTER IV

4. MODELLING AND CONTROL: PROPOSED SYSTEM

4.1. Architecture of the proposed system

Section 2.3.2 has presented the possible architectures for SST microgrids in the literature. The preferred architecture selected for the proposed system is Type V (as referred in Section 2.3.2) with a modification. Type V in Figure 2-5 has multiple zonal SSTs with AC/DC MGs. This architecture is ideal for large regional networks. The 400 m long feeder (feeder no 2); the system under study, is not fairly a large network but, had to employ the Type V architecture due to the SST capacity limitation in the design. Thus, the proposed system for the feeder 2 was designed with a distribution transformer along with the zonal SSTs. The developed SST is a low power (25 kVA) model and 3 zonal SSTs were employed to cater a 75 kVA maximum demand. Zones were based on both the geographical location of the customers and the solar PV generation.

Figure 4-1 depicts the feeder 2 and the distribution of solar PV along the 13 poles. Every pole has a loading level calculated based on the demand data taken from smart meters. This system is separated into 3 zones such that the maximum demand of each zone does not exceed 25 kVA (25 kVA is the designed capacity of single SST). The availability of solar PV for the three zones was also considered. The proposed system is shown in Figure 4-2. The distribution transformer is placed at the PCC of the grid and the feeder. Three parallel SSTs interface the zonal microgrid to the main grid. Each SST has a DC port and an AC port. Hence, AC and DC distribution lines supply power from the SST to each zone. The DC bus creates the DCMG since it has DC loads and solar PV generation. Moreover, the AC bus is connected with the diesel generator and AC loads to create the ACMG. The loading levels of each pole in Figure 4-1, is converted into AC and DC loading assuming Sri Lankan domestic customers have 50% DC loads. Each SST has a centralized battery storage, which is needed for the islanded operation of the microgrid. Solar PV at each pole was not changed.

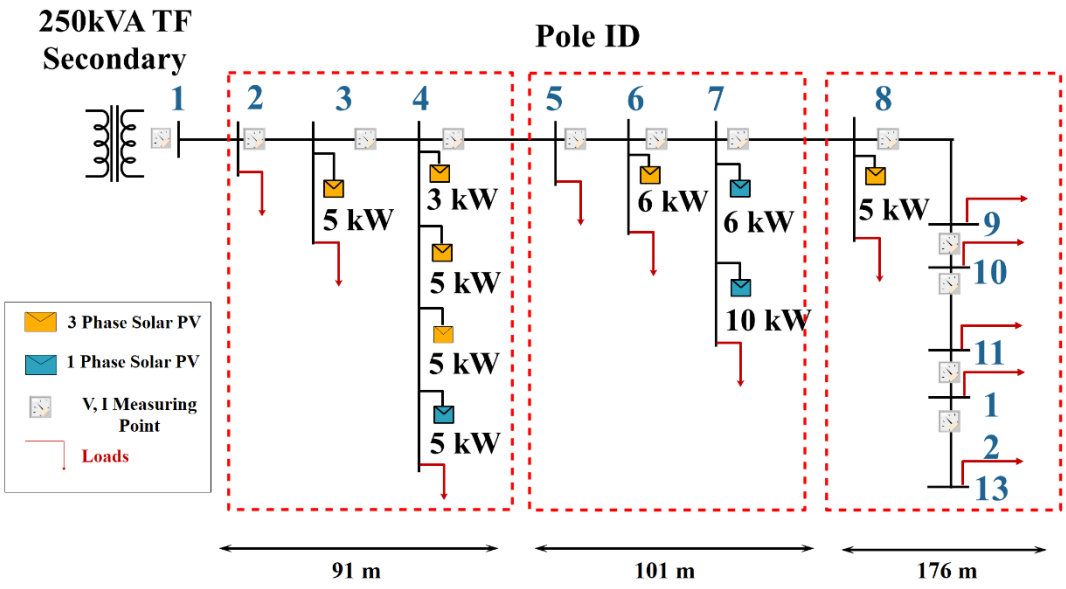


Figure 4-1: Existing feeder

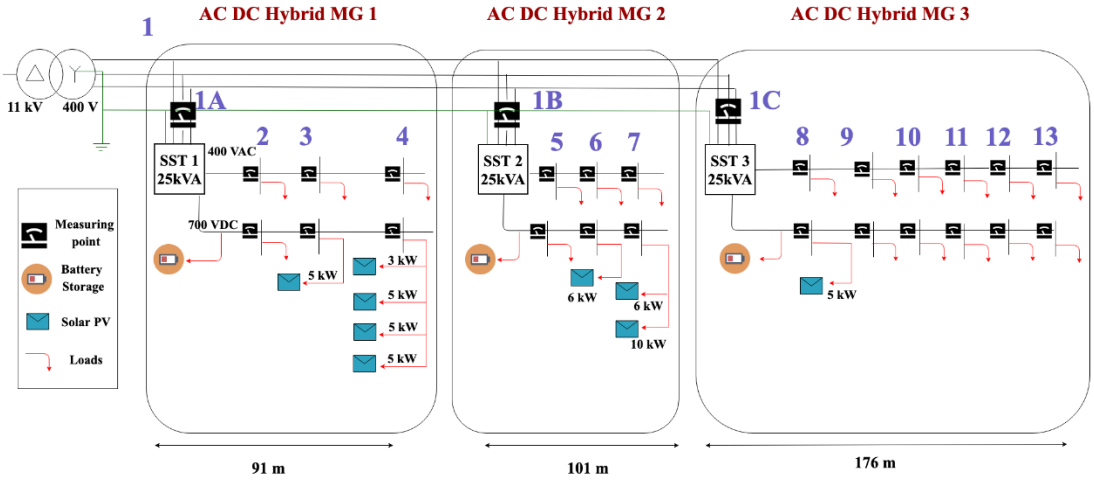


Figure 4-2: Architecture of the proposed model

The system parameters of the proposed system and each SST are given in Table 4-1. Each SST consists of a battery storage, AC/DC generation and AC/DC load. Solar PV capacities remain the same as in the existing system for the comparison. Refer Annex C for the Simulink models of the SST.

Table 4-1: System parameters

System Parameters		Single SST Parameters			
			SST 1	**SST 2**	**SST 3**
Single SST Capacity	25 kVA	Max Demand	23.7 kVA	17 kVA	12.6 kVA
System capacity	25 x 3 (75) kVA	ACMG Demand	14.2 kVA	9.8 kVA	7.2 kVA
Max Demand	60 kVA	DCMG Demand	11 kW	8.5 kW	6.5 kW
Feeder Length	400 m	DC Bus voltage	700 VDC		
Installed Solar Capacity	45 kW	AC Bus voltage	230V/400 VAC		
Earthing t/f	400V /400 V, Dy11, 15kVA	No. of Dc Buses per SST	2		

4.2. Distribution transformer

The distribution feeder interfaces the grid at the 11,000/ 400 V distribution transformer. A MATLAB two winding transformer was used with the specifications presented in Table 4-2. The distribution transformer data and calculations were obtained from [47].

Table 4-2: Distribution transformer parameters

Parameter	Value
Winding configuration	Dy11 | 3 limb core type
Nominal power and frequency (kVA, Hz)	250 | 50
Winding 1 parameters (V_{1L-L} RMS, R_1 pu, L_1 pu)	11000 | 0.0078002 | 0.020889
Winding 2 parameters (V_{2L-L} RMS, R_2 pu, L_2 pu)	400 | 0.0078002 |0.020889
Magnetization resistance (R_m pu)	565
Magnetization inductance (L_m pu)	107

4.3. Single SST System: Design and control

The design and control of a single SST will be discussed in this chapter. The SST 1 design considerations and related calculations will be presented in this section. The SST 2 and SST 3 have been configured to match the loading levels of the microgrid 2 and 3 respectively. The general SST is depicted by Figure 4-3.

The next sections will discuss the design considerations and the control schemes of the single SST. The discussion includes AC-DC converter, DC-DC converter, DC-AC inverter, DCMG and the ACMG.

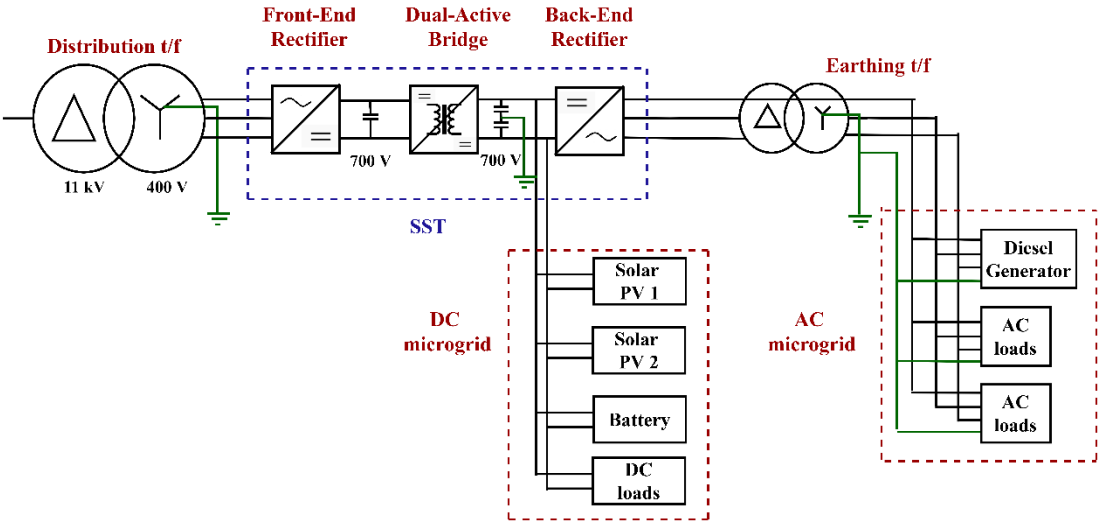


Figure 4-3: Single SST model

4.4. SST Stage 1: AC-DC Converter

The three phase AC-DC converter operating under PWM modulation is the first stage of the SST [19]. The lock diagram of the converter is shown in Figure 4-4. As the first stage of the SST, the converter is responsible for the voltage regulation of the MVDC bus of the SST and maintaining high power factor and low harmonic content at the input. For the accommodation of AC/DC hybrid microgrid with DRER and ESDs, the converter should have the following features:

- Bidirectional power flow
- Voltage source type
- High power factor

The distribution transformer output is connected to the converter bridge through simple L filter. Output of the converter has a capacitor filter to eliminate high frequency components from switching [19].

The AC-DC converter control is based on i_d-i_q current control which is discussed in detail in section 3.1.2.2. The $\boldsymbol{i_d}$ component is responsible for active power component and $\boldsymbol{i_q}$ for reactive power. In order to maintain a high power factor $\boldsymbol{i_q}$ is maintained at

zero. In this way, the reactive power is controlled. The control objectives of the controller were to maintain the (i) MVDC bus voltage and a (ii) high power factor.

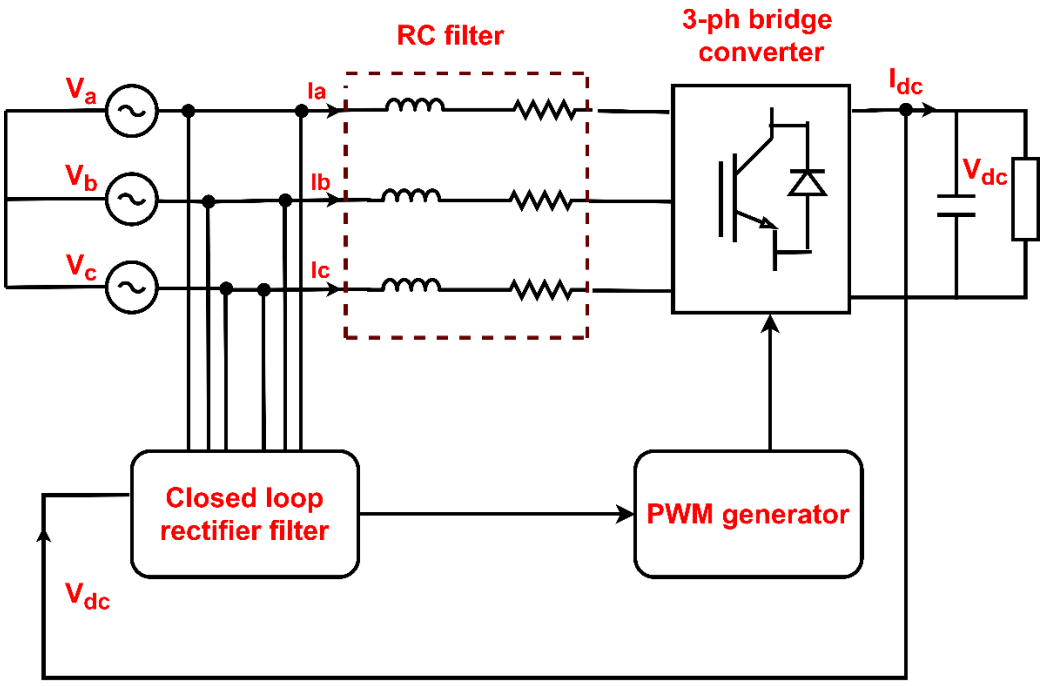


Figure 4.4: Block diagram of three phase AC-DC converter

Therefore, the controller should have a current controller to maintain the high power factor and a voltage controller to maintain the MVDC bus voltage. Figure 4-5 depicts the controlling diagram of the AC-DC converter. Let the input current and the voltage to the SST be $\boldsymbol{I_{abc}}$, $\boldsymbol{V_{abc}}$ and the medium voltage DC bus parameters be $\boldsymbol{V_{dc}}$ and $\boldsymbol{I_{dc}}$. To maintain the dc bus voltage, $\boldsymbol{V_{dc}}$ is taken as input and controlled with the reference $\boldsymbol{V_{dc}^*}$, which is 700 V. This voltage control loop also generates the d-axis current ($\boldsymbol{I_d^*}$) for the active power control across the rectifier. In order to maintain a unity power factor at the output of the rectifier, q-axis reference current ($\boldsymbol{I_q^*}$) is made zero. The PLL is used to lock the current phase angle and thereby accomplish the abc-dq transformation. The controlled outputs are converted back to abc reference and fed to the PWM generator. Figure 4-6 depicts the developed controller in MATLAB.

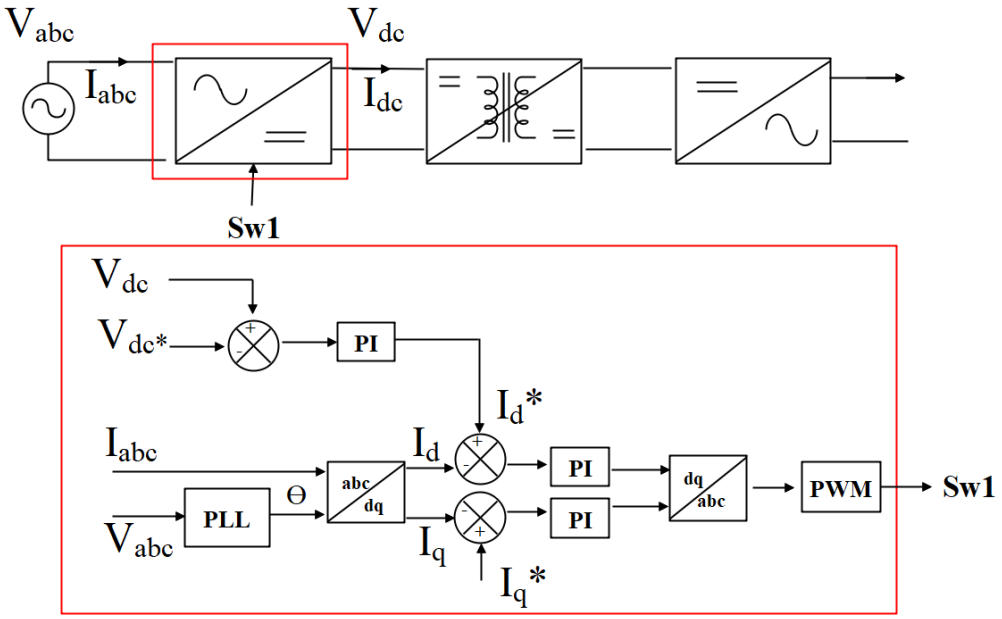


Figure 4-5: Current and voltage controller for the AC-DC converter

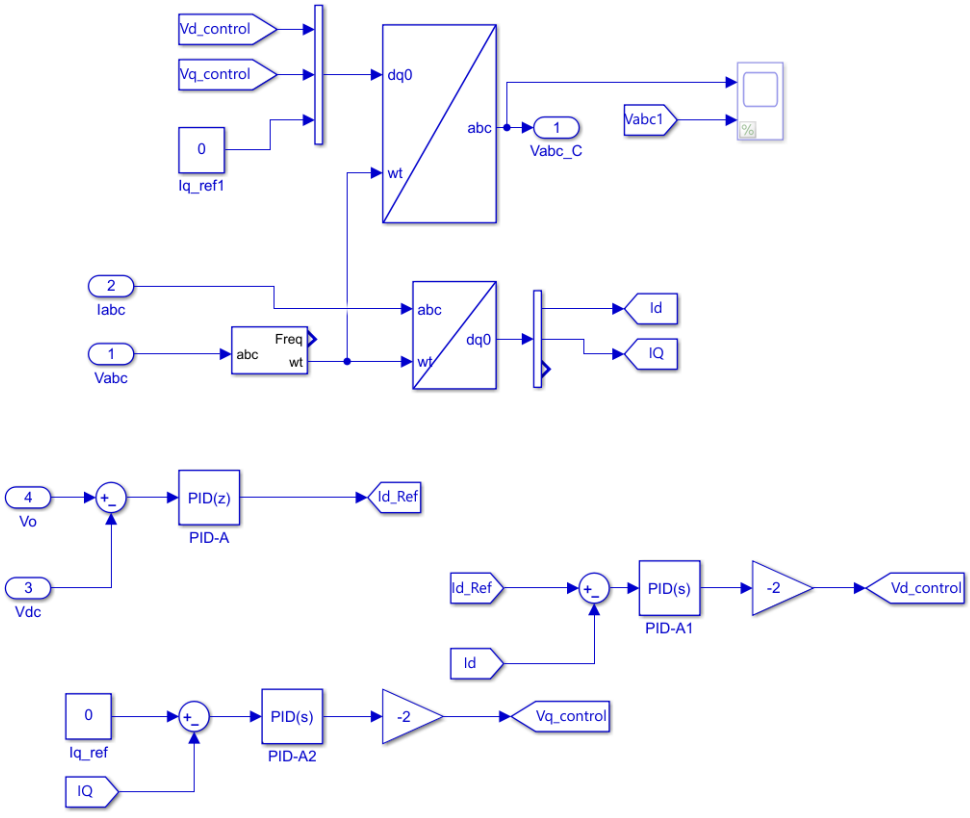


Figure 4-6: Modelled controller implemented in MATLAB

4.5. SST Stage 2: DC-DC Converter

The DAB was preferred for the DC-DC converter stage in the proposed design as explained in section 2.3.1. The DAB is comprised of semiconductor devices (IGBT + diode switches), an HFT, energy transfer inductor, and dc-link capacitors. The converter is symmetrical with identical primary and secondary bridges, hence capable of bidirectional power flow control, which is the main requirement for connecting with microgrids.

4.5.1. HFT

The HFT in the DAB has two major functions. (i) voltage transformation from the input MV to a LV (ii) Isolation. The IGBT switches in the DAB are usually designed to operate with 50% duty ratio. The bidirectional power flow of the DAB, which is achieved by controlling the phase shift of the two voltages in the DAB. The power flow equation is given by equation (4.1). The maximum power output is obtained at $\theta = \frac{\Pi}{2}$ by differentiating (4.1). The rated power of the DAB was designed to 25 kW catering the power requirement of the microgrid. The main design considerations of the DAB are:

- Selection of an appropriate switching frequency (***f***)
- leakage inductance (***L***)
- phase shift (θ) for the rated power of the DAB

$$P_{out} = \frac{V_{in}V_{out}\theta}{2\pi f_{sw}L}\left(1 - \frac{\theta}{\pi}\right); \qquad 0 < \theta < \frac{\Pi}{2} \tag{4.1}$$

The increased operating frequency (***f***) reduces the winding window area ($\boldsymbol{A_w}$) and the core area of the transformer ($\boldsymbol{A_c}$) without increasing the current density (***J***) and maximum core flux density ($\boldsymbol{B_m}$). In high power density applications (***S***), if not for the size and volume reduction, higher currents are required, and this relation is expressed as given in equation (4.2) [59]

$$A_w . A_c \propto \frac{S}{B_m . f_{sw} . J} \tag{4.2}$$

This makes a less weight and volume option in the transformer applications. However, the losses in the system increases with high frequency. The increased frequencies

increase the system losses (both converter and HFT) and ultimately in the cooling system [59]. Therefore, the optimizing of the frequency and the size of the transformer based on core and winding material is a major concern in the practical implementation of the SST [59]. However, in this design an initial frequency of 20 kHz was selected as the switching frequency based on the trade-off of volume/ weight and efficiency [60]. Many typical IGBT applications employ 20 kHz is another reason to choose the particular frequency. For optimal operation, the maximum phase shift of the dual active bridge should be around 30% of the total operating range [61]. Hence, $\boldsymbol{\Theta}$ was selected as 27º. The design parameters are presented in Table 4-3.

Table 4-3: Parameters for the design of DAB

Parameter	Symbol	Value
Output power of the DAB	$\boldsymbol{P_{out}}$	25 kW
Input voltage to the DAB	$\boldsymbol{V_{in}}$	700 VDC
Input voltage of the DAB	$\boldsymbol{V_{out}}$	700 VDC
Switching frequency	$\boldsymbol{f_{sw}}$	20 kHz
Leakage inductance	$\boldsymbol{L}$	63.21 µH
Phase shift	$\boldsymbol{\theta}$	27º

4.5.2. DAB Operation

To analyse the DAB operation, it is important to derive the switching operation of single H-bridge which is shown in Figure 4-7. Each switch of one leg is turned on and off in a complementary fashion, causing the voltage at the phase leg output ($\boldsymbol{V_{OUT}}$) to switch between the upper and lower voltage rails ($+\boldsymbol{V_{DC}}$) and ($-\boldsymbol{V_{DC}}$). Here, S4 = $\overline{S1}$ and S3= $\overline{S2}$. The H-bridge has four possible states, depending on its switches (S1, S2, S3, S4). The truth table of Table 4-4 describes these states, and shows that they produce three possible output voltage levels as positive ($2\boldsymbol{V_{DC}}$), negative ($-2\boldsymbol{V_{DC}}$) and zero.

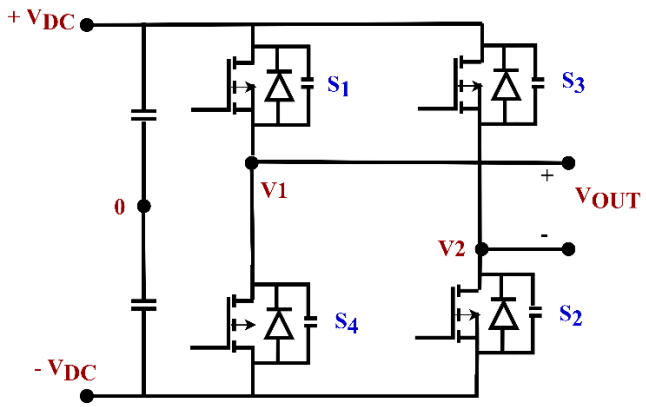


Figure 4-7: H bridge converter

Table 4-4: H bridge truth table

S1	S2	V1	V2	V_{OUT}
0	0	-VDC	+VDC	-2VDC
0	1	-VDC	-VDC	0
1	0	+VDC	+VDC	0
1	1	+VDC	-VDC	+2VDC

This results in the Table 4-4, and can be summarized by the equation (4.3). The switches in the H bridge are switched with 50% duty cycle with 180º offset to get square wave output. Since the switching signals are time varying, a time dependent equation is derived as in equation (4.4).

$$V_{OUT} = 2V_{DC}\{S1 - S2\} \qquad (4.3)$$

$$V_{OUT}(t) = 2V_{DC}\{S1(t) - S2(t)\} \qquad (4.4)$$

The modulation principles of the H-bridge can thus be extended to demonstrate the DAB converter operation. Each bridge of the converter is modulated from PSM, as illustrated in Figure 4.7. The resulting DAB output voltage waveforms ($\boldsymbol{V_{primary}(t)}$ & $\boldsymbol{V_{secondary}(t)}$) can be described in terms of the converter switching functions as given in equation (4.5) and (4.6). The DAB operation with its switching signals are shown in Figure 4-6. The used notations are as explained above.

$$V_{primary}(t) = V_{in}(t)\{S1(t) - S2(t)\} \qquad (4.5)$$

$$V_{secondary}\,(t) = V_{out}(t)\,\{S5(t) - S6(t)\} \qquad (4.6)$$

The two bridge output voltages $\boldsymbol{V_{primary}(t)}$ & $\boldsymbol{V_{secondary}(t)}$) (t) are offset from each other by a phase difference **Θ** as shown in Figure 4-8 (a). This causes a non-zero net voltage VL to appear across the 63.21 μH inductor, which in turn causes the current transformer current to flow. The inductor acts as an energy buffer to absorb the excess power. Hence, the net power flows from the leading bridge to the lagging bridge.

Using the Figure 4-8(b), the maximum inductor current can be determined. The current slope can be given by,

$$\frac{\Delta i}{\Delta t} = \frac{V_L}{2.\Pi f_{sw} L} \qquad (4.7)$$

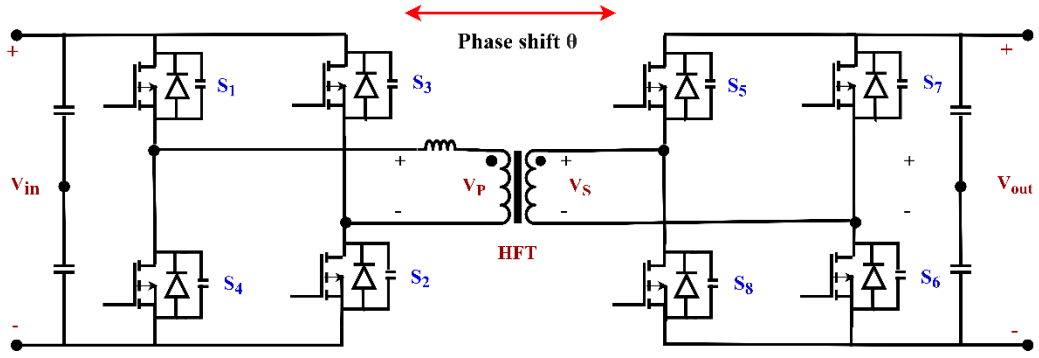
From, 4.4 it can be shown that the voltage on the inductor is double the voltage value of the input value during the phase shift. Observing Figure 4-8(b), this voltage value is bit lower due to the field weakening. Hence,

$$\Delta i = \frac{2V_{sec}\Theta}{(2\Pi f_{sw})L}; \quad \Delta t = \Theta \qquad (4.8)$$

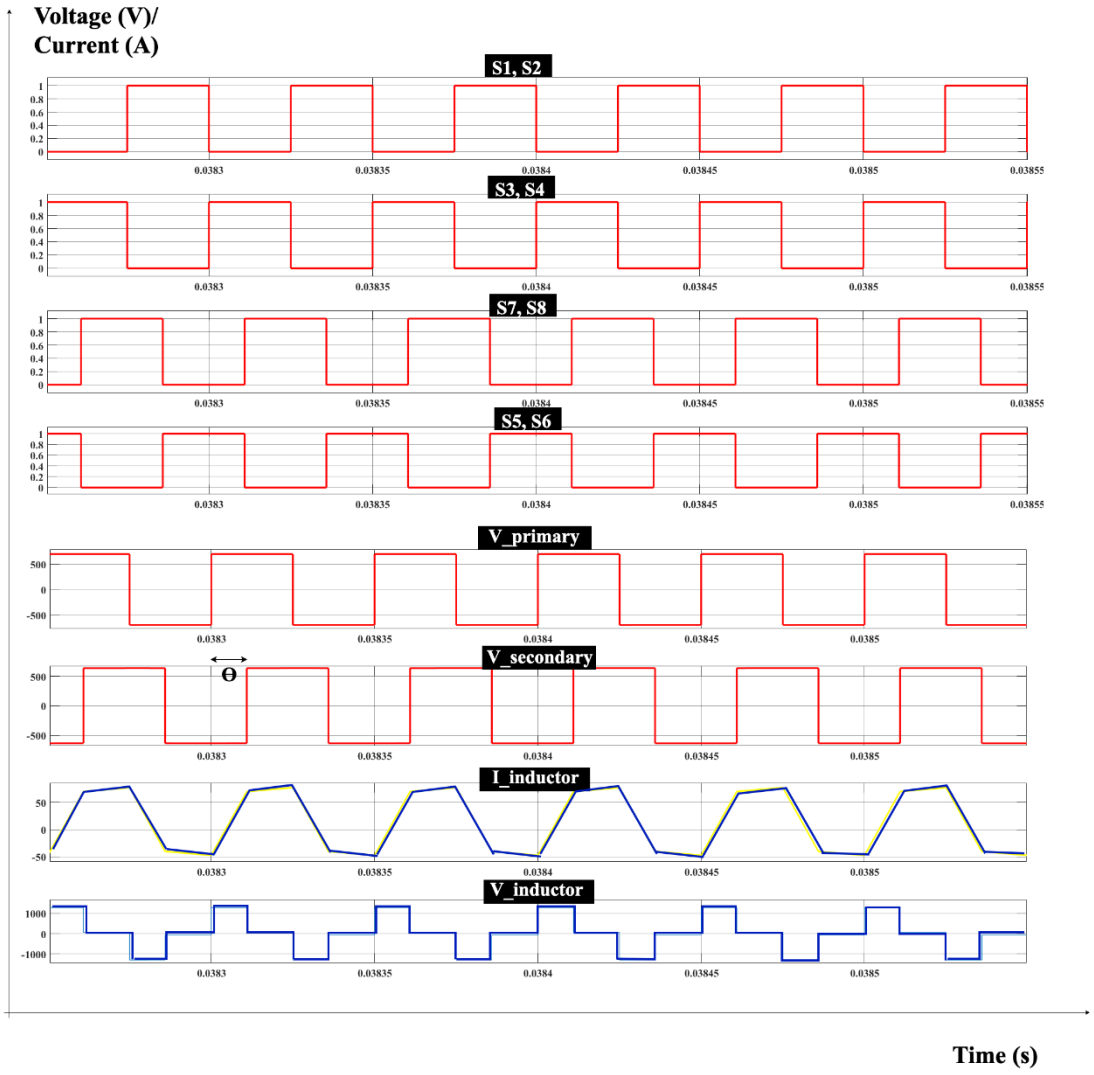
The maximum inductor current occurs when $\Theta = \frac{\Pi}{2}$. For steady state current varies from negative maximum to positive maximum. Hence, the variation of current is double the maximum value of the current.

$$I_{max} = \frac{V_{sec}}{4 f_{sw} L};\ I_{max} = \frac{\Delta i}{2} \qquad (4.9)$$

The maximum current is important in selecting the components such as DC link capacitor and filter inductances. The calculated maximum peak current from (4.9) is 138 A.



(a)



(b)

Figure 4-8: (a) Switching signals for theDAB (b)Operating waveforms of DAB at rated power simulated in MATLAB

4.5.3. DAB Controller

The MATLAB implementation of the DAB, the controller and the gate pulse generator are shown in Figure 4-9.

4.5.3.1. LVDC Bus voltage controller

In the SST, the DAB converter maintains the LVDC bus voltage at 700 V. The DAB input voltage is controlled by the first stage AC-DC converter and is considered constant for the DAB design [19]. The output voltage of the DAB varies with the phase shift between the two switching waveforms to provide the required power given by the equation (4.1). Therefore, the controller acts in the angular displacement ($\boldsymbol{\Theta}$) between the primary and secondary voltages to ensure the LVDC output bus regulation and permits the variation in power flow direction [19]. The IGBT switches of the bridges are operated with a displacement in order to guarantee the LVDC bus voltage at 700 VDC and the bidirectional power flow [19]. This control diagram is shown in Figure 4-10.

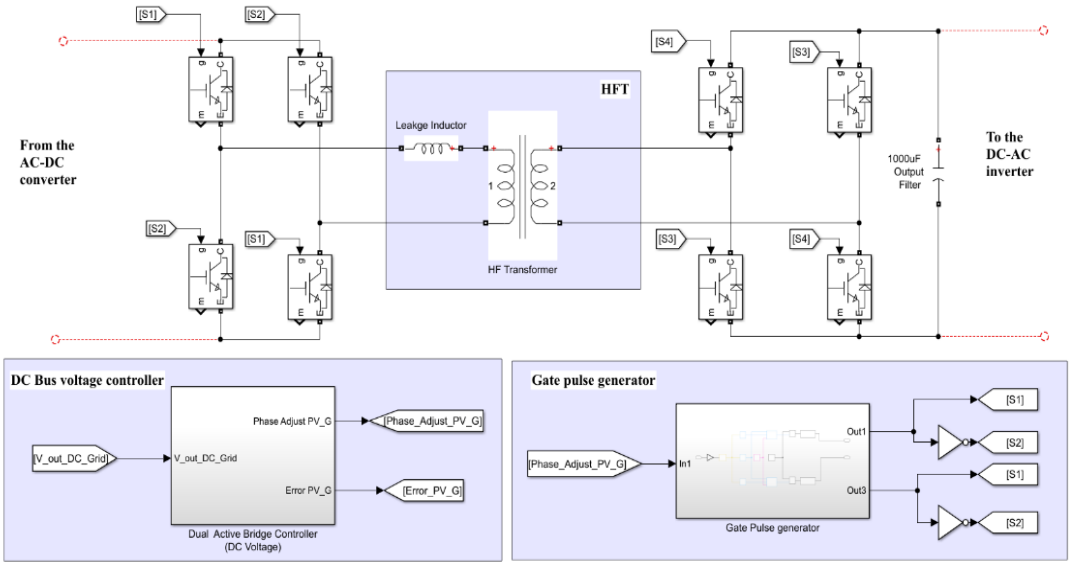


Figure 4-9: MATLAB implementaion of the DAB

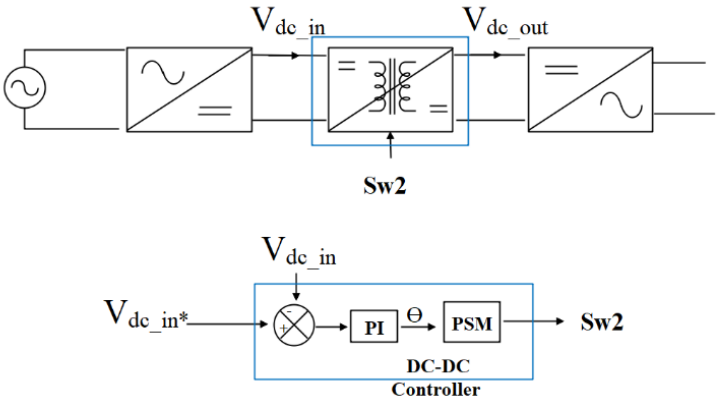


Figure 4-10: DC-DC converter controller

4.5.3.2. Gate pulse generator

The gate pulse generator drives the IGBTs of the DAB to provide the required phase shift. The developed gate pulse generation scheme is shown in Figure 4-11 [47]. The phase shift generated was converted to a time delay and was triggered at the start of every switching cycle using zero order hold block. The negative phase shifts was given to the MVDC side of the DAB (S1, S2) while the positive phase shifts were given to the LVDC side of the DAB (S3, S4). The NOT gate was used to generate the complement of the output signal of the second IGBT of one arm of the bridge. The phase shift was limited to $(\mathbf{0} - \frac{\boldsymbol{\Pi}}{\mathbf{2}})$ using the variable time delay block.

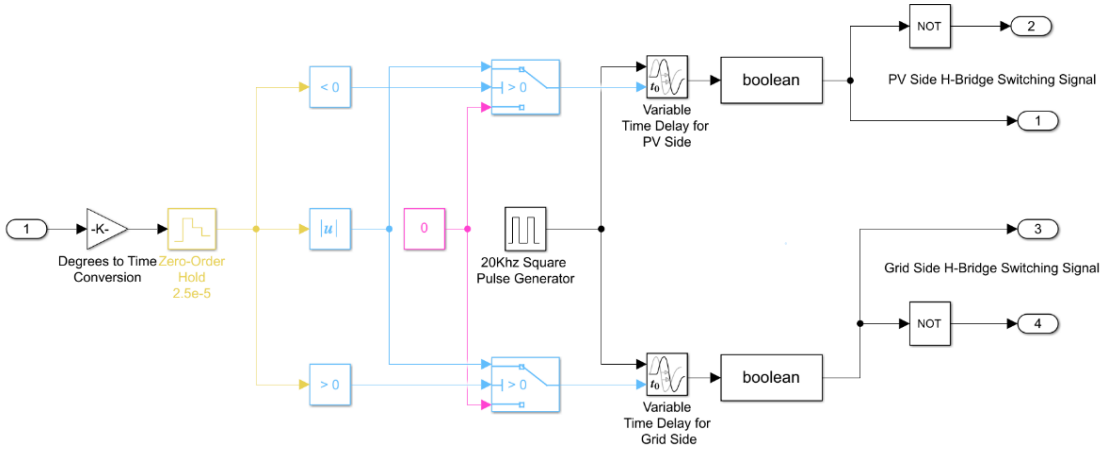


Figure 4-11: Gate pulse generator

4.5.3.3. DC Output Capacitor selection

The DC bus capacitance of the DAB should be designed to handle the ripple voltage. Following the procedures explained in [62], first step is to find the maximum peak to peak ripple as equation (4.10).

$$I_{p-p} = \frac{V_{sec}}{2f_{sw}L} \qquad (4.10)$$

Applying the capacitor equation to find the ripple in the voltage shown in equation (4.11),

$$dV = \frac{i_c}{C}dt \qquad (4.11)$$

The current in the capacitor is the ripple in the inductor. Therefore the voltage deviation can be given as equation (4.12)

$$dV = \frac{V_{sec}}{2f_{sw}LC}dt \qquad (4.12)$$

Integrating, 4.11 and applying $\Delta t = 0.5t$ (considering 50% duty cycle) and f=1/t yields to equation (4.13);

$$\Delta V = \frac{V_{sec}\,\Delta t^2}{4f_{sw}LC} \qquad (4.13)$$

Since the maximum current appears at $\theta = \frac{\pi}{2}$ which is 0.25 of the period.

$$V_{p-p} = \frac{V_{sec}}{64f_{sw}{}^2LC} \qquad (4.14)$$

This relationship of voltage ripple was plotted against the DC link capacitance in Figure 4-12. It can be seen that increasing the capacitance does not significantly improve the ripple voltage. Increasing capacitance implies high cost. Hence, 330 µF commercially available electrolytic capacitor was employed expecting a ripple voltage of 1.25 V.

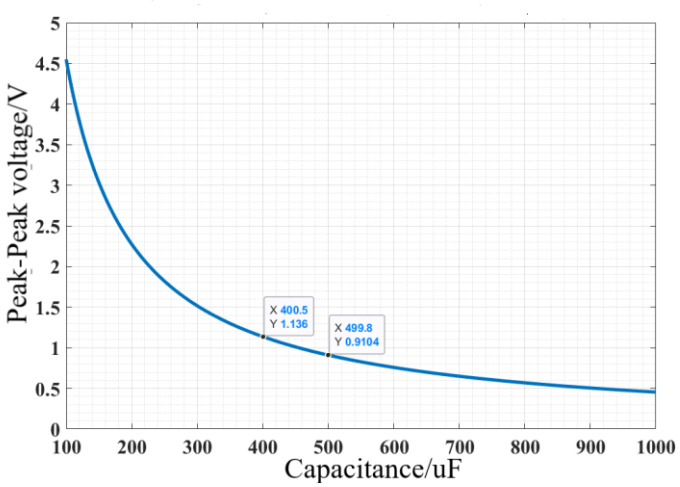


Figure 4-12: Voltage ripple Vs capacitor value of the DAB

In selecting the capacitor, it is necessary that to investigate the maximum current the capacitor can withstand which was calculated as 138 A. From Figure 4-13 the expected peak to peak ripple voltage has been obtained as 1 V.

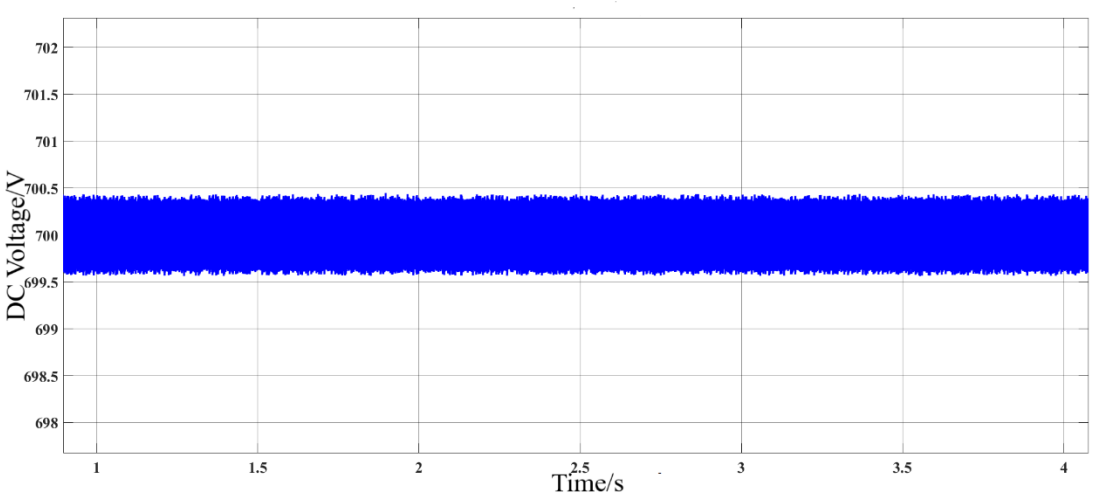


Figure 4-13: Output voltage of the DAB

4.6. SST Stage 3: DC-AC inverter

The DC-AC voltage source inverter is the last stage of the SST, which converts the DC bus voltage to the three phase AC voltage. The implemented model is shown in Figure 4-14. The full bridge converter with IGBT switches are adopted, which generate

the three-phase voltages shifted by 120°, arising from the SPWM. The input to the inverter, the LVDC voltage of 700 VDC is regulated by the DAB and is assumed to be constant to the inverter. The control objective of the inverter is to generate and regulate the output AC voltage measuring the real time power. Since the inverter voltage output is modulated, an LC filter is necessary to filter the high frequency components generated from switching. The voltage control is made based on the filter electrical quantities (voltage and current). The inverter output voltage is fed to the outer loop and converted to the dq components. The PLL is used to keep track of the phase angle. Depending on the loads connected to the ACMG, the current drawn from the inverter varies hence, the power output is varied. This power is tracked from the controller and the d axis current is produced similar to the AC-DC converter controller. The d axis current is converted to abc components and the gate pulses to the IGBT are generated. The converter controller implemented in MATLAB is shown in Figure 4-15.

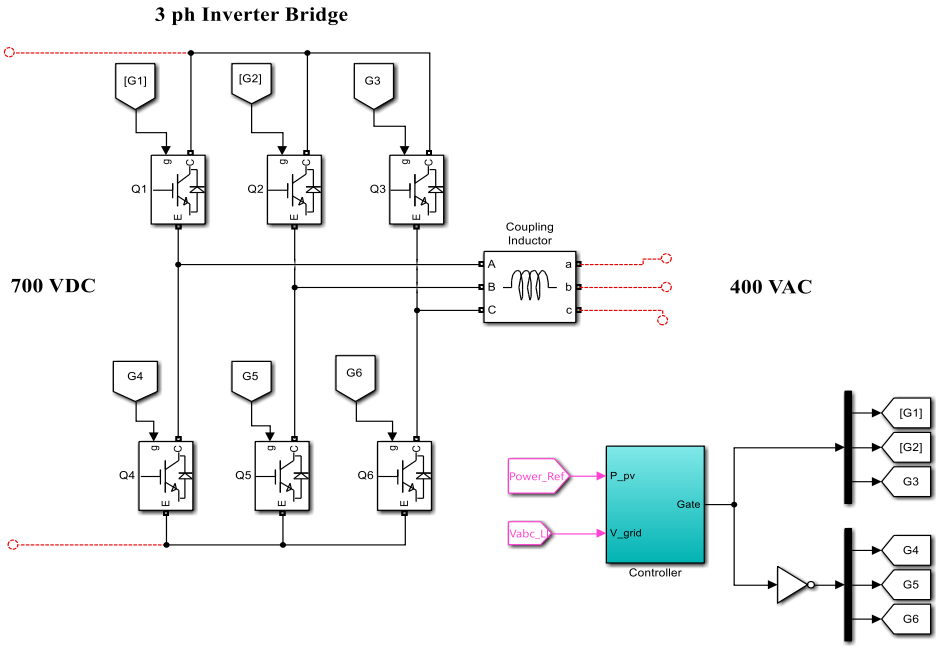


Figure 4-14: Modelled 3 phase inverter

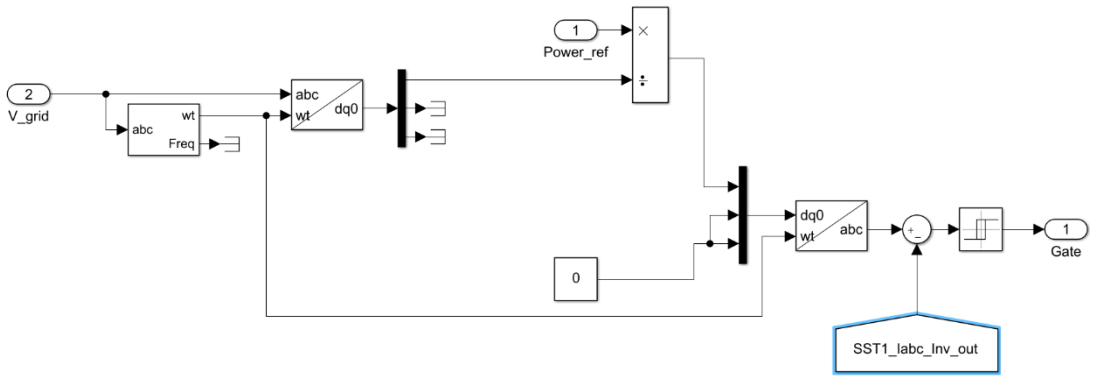


Figure 4-15: DC-AC converter controller

4.7. Grounding configuration

Grounding electric power systems has many approaches and result in various performance. Grounding is used for the protection of personnel and equipment and the detection of ground faults Sri Lankan network has a T-T grounding system. The distribution transformer secondary side has a direct earth connection [77]. At the consumer side, protective earth is provided by a local earthing electrode [77].

The DCMG can be ungrounded, high impedance or low impedance grounded. Ground connection point can be either one of the positive or negative poles or the midpoint of the DC bus [63]. For the SST based DCMG grounded connection can be achieved by either way. For this model DC bus mid-point grounding is selected for the DCMG grounding to reduce the touch voltage (from 700 V to 350 V) and to provide an extra voltage level to the DC network.

In grounding the AC distribution network, three phase Y connected network readily provides a neutral connection, which can be grounded. In SST ACMG, the SST isolation and the DC-AC converter output provides no neutral connection. Hence, a grounding transformer is used to obtain the neutral point of the ACMG [64]. The proposed grounding system is shown in Figure 4-16.

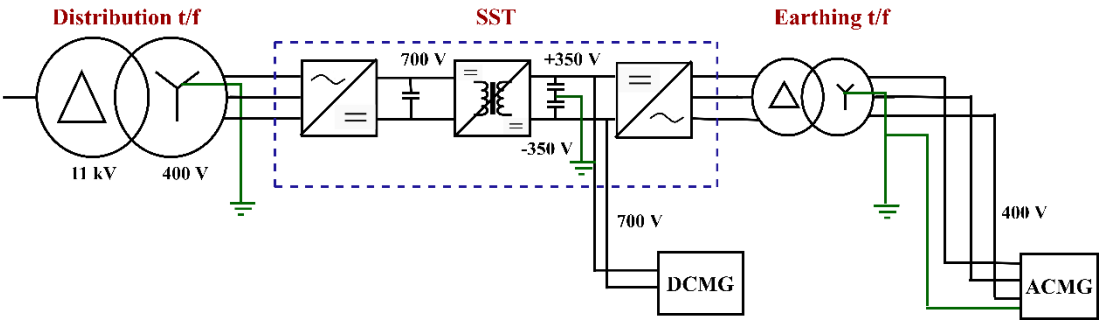


Figure 4-16: Proposed grounding system

4.8. DCMG

The DCMG consist of the solar PV, DC loads and energy storage. The solar PV and DC load modelling and controlling was discussed in Section 3.1. This section presents the details of ESD and the designed energy management system.

4.8.1. DC distribution line

Since the proposed system is developed under the concept of supplying of both AC and DC distribution network it is equally important to plan the DC distribution line. Both safety and efficiency has to be considered in deciding the DC distribution voltages. The voltage drop and power loss in a DC line can be calculated using equations 4.15 and 4.16 [65]. Accordingly, power requirement and line resistance being constant, a smaller voltage drop and smaller power loss is achieved only by selecting a higher DC voltage for the distribution.

$$\Delta V_{DC} = 2 \times R \times \frac{P}{V_{DC}} \qquad (4.15)$$

$$\Delta P_{DC} = 2 \times R \times \frac{P^2}{{V_{DC}}^2} \qquad (4.16)$$

Nominal voltage of 48 VDC has been chosen as the best voltage for LV distributed power system for data and communication centers [66]. 380 VDC is the accepted voltage level among many entities establishing facilities with DC distribution due to its high efficiency, reliability, and reduced copper costs. However, up to 550 VDC is used by commercial organizations like ABB and Siemens for DC distribution [66].

In the proposed system, DC bus mid-point grounding configuration has allowed two DC voltage levels; 350 VDC and 700 VDC. Considering all the factors like efficiency, protection and reliability, 350 VDC is the most suited as the distribution voltage for the DCMG. Since the distribution feeder spans a distance of 400 m, and given that the only one ESD is located for the DCMG, to reduce the voltage drop and to reduce losses 700 VDC was used.

In designing a DC micro grid, the cable size must be chosen carefully so that the voltage falls within the allowed band throughout the full feeder length and maximum current of the bus. In the case that the bus length is too long to equalize the voltage, ESD need to be installed separately in the DC micro grid.

In selection of the DC cables, the maximum current of the DC distribution was calculated. Considering a maximum demand of 12.5 kW, the 700 VDC distribution system must be designed to cater an amperage of 21 A (safety factor of 1.2). Unlike DC cables, AC cables are subjected to skin effect; hence, at a particular voltage, the resistance of a cable for DC is less than that of for AC. Therefore, an amperage through a DC cable will generate slightly less amount of heating than the AC current through a cable. Considering the current carrying capacity of 17A and 2% of voltage drop for 400 m long feeder, the 25 mm^2 cable was selected for the conductor. According to ACL catalogue for power cables [67] the cables are designed for 600 V-1000 V. Hence, the cable R=0.5 Ω/km.

4.8.2. ESD

An ESD of a microgrid consist of the battery, charging/discharging controller and a DC-DC converter to match the bus voltage. Basic Requirement of the ESD in a microgrid is to store energy at a time of surplus and re-dispatch when needed and will ultimately improve system reliability. For the proposed ESD, the battery model in MATLAB was employed. The battery voltage was chosen as 220 V and has to be connected to a DC-DC converter such that it can be connected to the 700 VDC bus as shown in Figure 4-17. Since the scope of the thesis is limited to grid connected mode, the controller was designed focusing the control of charging current.

Four possible BES technologies are given in MATLAB; lead acid, NiCd, Li-ion, and NaS. Lithium-ion battery found economically more viable than lead-acid battery. Apart from the costs, Li-ion batteries offer additional advantages like reduced maintenance, more flexibility in SOC, fast charging rate, smaller volume and longer cycle life. Hence, lithium-ion batteries are recommended over other technologies as a viable solution in applications of future electric power systems [67] [68].

In order to calculate the battery capacity (see equation (4.17)), it was assumed that the battery has to deliver rated output power (25 kW) for a maximum time period of four hours. Considering battery voltage of 220 V, battery bank was designed by connecting five 48 V each battery cells in series.

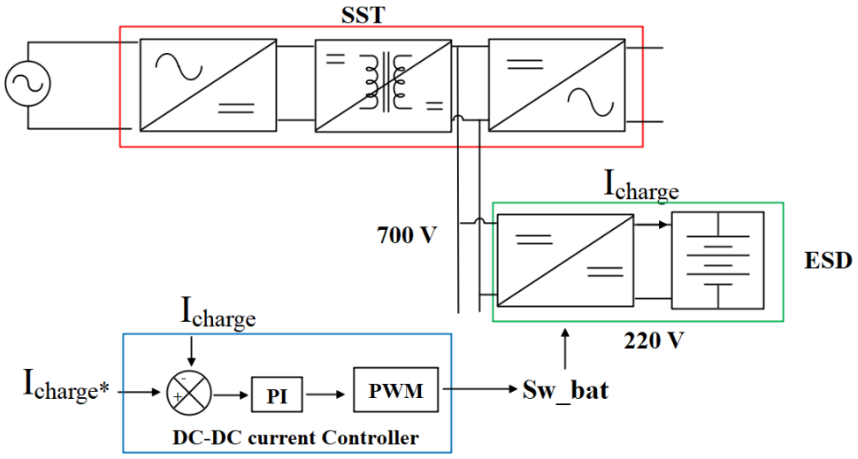


Figure 4-17: ESD block diagram and the voltage controller

$$\text{Battery Capacity} = \frac{\text{Maximum Power (W)x Total time(hrs)}}{Battery\ voltage\ (V)} \qquad (4.17)$$

$$\approx 400\ Ah$$

Single microgrid can run in islanded mode for four hours with a battery of 400 Ah. In considering the role of ESD in a microgrid, it is necessary to analyse the operating modes of a microgrid: grid connected mode and the islanded mode. The proposed power management algorithm for both modes are presented in Appendix D. However, the scope of the thesis is focused on the grid connected mode.

Constant-current/ Constant-voltage (CC/CV) controlled charging system is used to charge Lithium batteries. Constant current charging rate is the maximum charging rate, which the battery can tolerate without damaging the battery. Therefore, it is recommended that the charging method switches to constant voltage before the battery voltage reaches its upper limit. In the designed controller, only the constant current charging at 10 A is employed. Based on the DC-DC converter output current and the selected commercial Li-ion battery selected, 10 A was used [69]. The initial SOC of the battery was considered to be 50%. Figure 4-18 shows the Battery parameters at the charging mode. A constant current of 10 A (See Figure 4-18(c)), controls the terminal voltage of the battery (220 V). At t=0 s, charging starts and the SOC=50% and this image was captured at t=0.3 s to t=0.5s. The increasing of SOC over time is visible from the Figure 4-18(b). Terminal voltage at this instance is 219 V as can be seen in the Figure 4-18 (a).

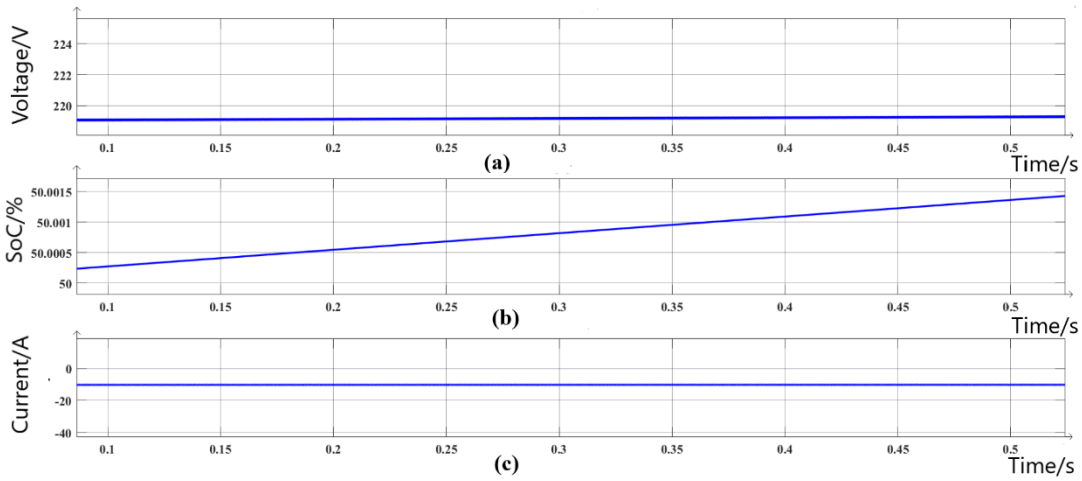


Figure 4-18: Battery charging waveforms (a) Battery voltage Vs time (b) battery SoC Vs time (c) Battery current Vs time

4.9. ACMG

The ACMG consist of a diesel generator, which represent the AC generation and three phase and single-phase AC loads. The loads are connected to induce a slight voltage unbalance, which replicate the existing system. Modelling of the LV network is presented in Section 3.1.1.

4.9.1. AC generator

In order to mimic the role of a distributed generation in the ACMG, a diesel generator has to be employed. A diesel generator set consist of a diesel engine, which is the prime mover and a synchronous generator. The simplified synchronous machine with the mechanical input, which was readily available in the MATLAB Simulink Power Systems Library was employed. Each phase of the electrical system consists of a voltage source in series with an RL internal impedance. The mechanical system is described by (4.18) and (4.19),

$$\Delta\omega(t) = \frac{1}{2H}\int_0^t (\tau_m - \tau_e)dt - K_d\Delta\omega(t) \qquad (4.18)$$

$$\omega(t) = \Delta\omega(t) + \omega_0 \qquad (4.19)$$

where $\boldsymbol{\Delta\omega(t)}$**:** is the speed variation with respect to speed pf operation, **H**: inertia constant, $\boldsymbol{\tau_m}$: mechanical torque, $\boldsymbol{\tau_e}$**:** electrical torque, $\boldsymbol{K_d}$**:** damping factor which represents the effect of damper windings, $\boldsymbol{\omega(t)}$: mechanical speed of the rotor, and $\boldsymbol{\omega_0}$**:** speed of operation. The machine parameters for 5 kVA diesel generator set was based on [70] and the manufacture's specification sheets [71]. The input parameters to the model were converted to per unit from the data obtained. The parameters used for the modelling are as tabulated in Table 4-5. Initial conditions were calculated based on 2,500 W generation. The generator output is shown in Figure 4-19.

Table 4-5: AC Generator parameters

Parameter	Value
Voltage	400 V
Power	5000 kVA
Frequency	50 Hz
Internal Resistance	1.62
Internal Reactance	0.05175 H
Inertia J	0.0923 kgm^2
Friction factor	0.009 Nms
Poles	2

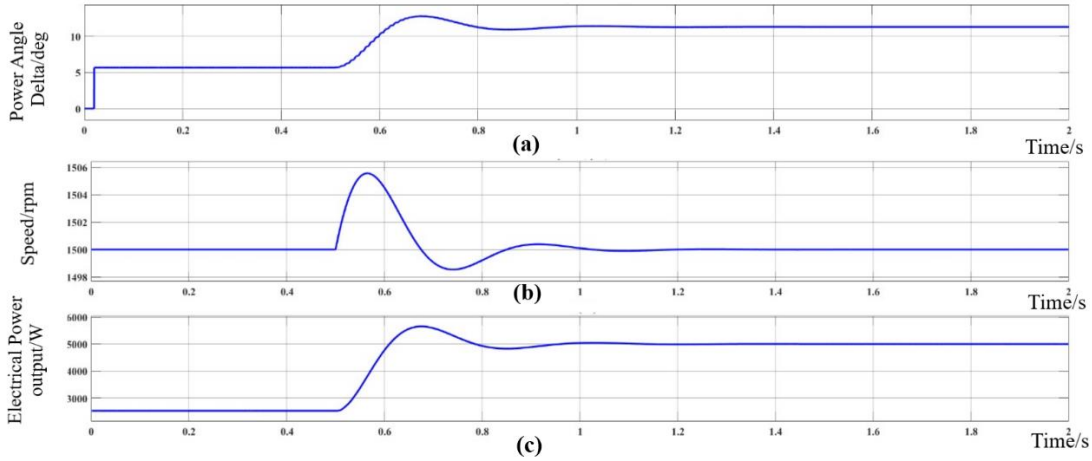


Figure 4-19: AC generator output waveforms (a) Power angle Vs time (b) Generator speed Vs time (c) Electrical Power Output Vs time

CHAPTER V

5. PERFORMANCE ANALYSIS OF THE PROPOSED SYSTEM

The performance of the proposed system was analysed such that it can be compared with the results of the existing system. The cases considered for the existing network was presented in two scenarios in Chapter 3, which concluded that higher distortion levels were resulted with 50 % of non-linear loads in the systems. Therefore, in this analysis, only the cases under Scenario 2 of Figure 5-1 was considered.

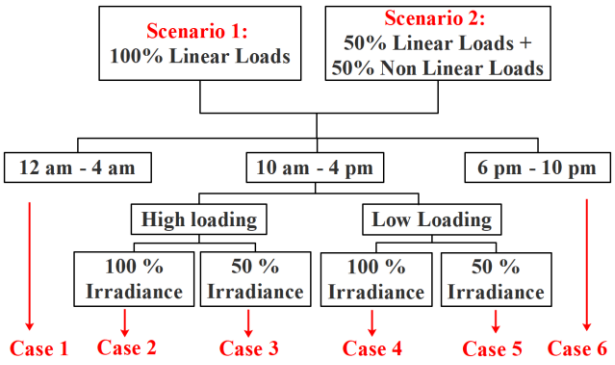


Figure 5-1: Cases studied for the proposed system

5.1. Power flow of the system

The DCMGs and ACMGs are constituted by the DRER, ESDs and loads. For these components to operate in a coordinated manner, a proper power management strategy must be established. The use of a communication network along the distribution feeder and a centralized controller will achieve this task. However, a communication failure can compromise the microgrid operation. On the other hand, distributed methods, such as DC bus signalling (DBS) confers higher reliability and a basic power flow management and can be incorporated in a hierarchical control structure, which can also provide optimal performance [28].

The proposed distribution system was designed to be analysed only in the grid connected mode. Therefore, the grid supplies deficit in the power requirements in microgrids depending on the load requirement of each SST. Individual SSTs are equipped with separate controllers that measure the real time power and can deliver

the required power to the loads. Also, a fraction of this power is provided by power generated in the AC/DC hybrid microgrid. The SST allows bi-directional power flow depending on the generation/load availability.

5.1.1. Power flow of single SST

This section presents how the power flow happens in a single SST microgrid. As explained in Chapter 4, the proposed SST controls only the active power flow by controlling the d-axis current. The DCMG power requirement is provided by the MVAC grid side and controlled by the SST. The active power required for the ACMG is provided by the grid side whereas the reactive power requirement is supplied by the LVDC capacitor bank. However, the active power flow is controlled at each stage of the SST. Development of a controller that estimates the reactive power that should be injected from the grid side based on the reactive power requirement is not under the scope of this thesis.

Active power utilization of a single SST under six different cases are presented. The SST 3 was selected to represent the results. The power flow values were analysed to observe the losses at each conversion stage to rectify the losses of the converters and the distribution network. Figure 5-2 depicts the symbols used for the power flow of a single SST. The power input to the AC-DC converter, DAB and the DC-AC converter are $\mathbf{P_{AC\text{-}DC}}$, $\mathbf{P_{DAB}}$, and $\mathbf{P_{DC\text{-}AC}}$ respectively. Input power to the ACMG and the DCMG are $\mathbf{P_{ACMG}}$ and $\mathbf{P_{DCMG}}$ respectively. The power output from sources (solar PV and the AC generator), storage device(battery) and the AC,DC loads are also depicted in the Figure 5-2. These values were obtained from the simulation to analyse the efficiency of each conversion stag. From the simulation, steady state power values for the Case 3 were obtained in graphs as shown in Figure 5-3. Similarly, for all the cases, steady state power values were tabulated in Table 5-1.

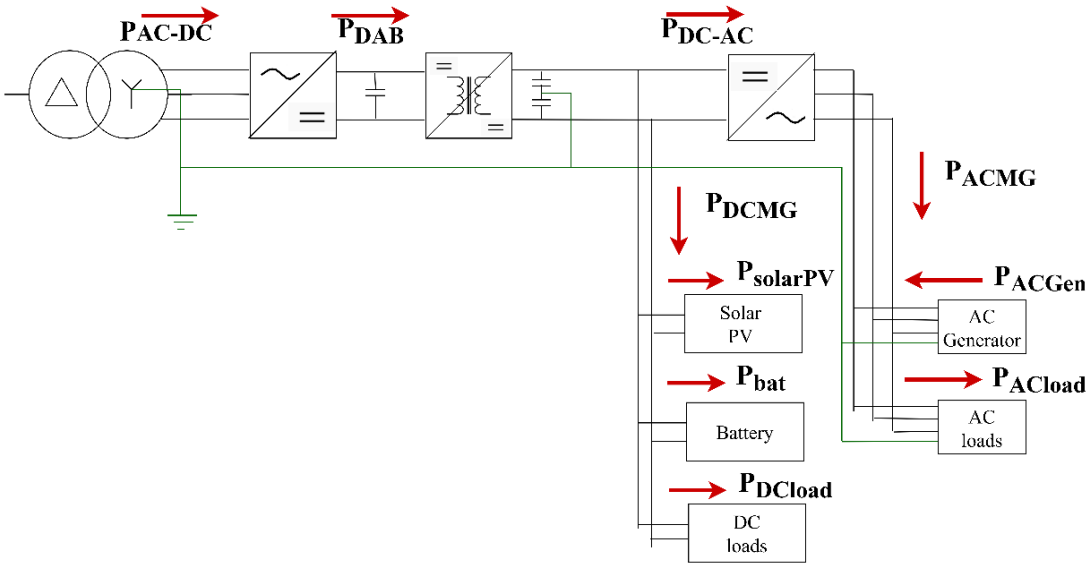


Figure 5-2: Power flow of a single SST

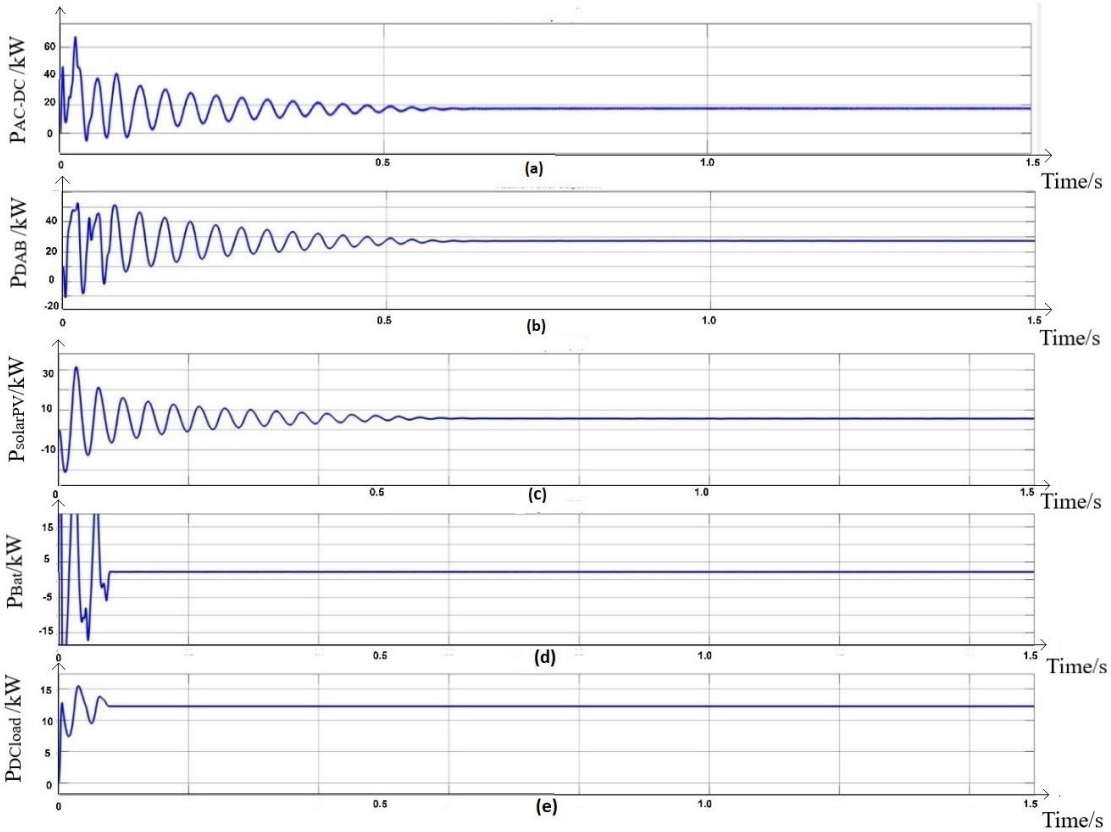


Figure 5-3: Power Vs time at SST 3 for Case 3 (a) Power input to the AC-DC converter, $P_{AC-DC,}$ (b) Power input to the DAB, P_{DAB} (c) Power output of the Solar PV, $P_{solarPV}$ (d) Input power to the Battery, P_{bat} (e) Output power of the DC loads,P_{DCload}

Table 5-1: Power flow values in different cases of a single SST

P/kW	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
P_{AC-DC}	1.330	20.449	20.743	1.135	1.112	32.430
P_{DAB}	1.266	20.008	20.100	1.089	1.067	31.732
P_{DCMG}	4.859	11.230	11.270	1.921	1.904	19.972
P_{bat}	2.500	2.500	2.500	2.500	2.500	2.500
$P_{solarPV}$	0.000	-5.000	-5.000	-5.000	-5.000	0.000
P_{DCload}	1.800	12.500	12.500	4.200	4.200	15.300
P_{DC-AC}	-3.653	8.386	8.378	-0.888	-0.888	11.108
P_{ACMG}	-3.424	8.025	8.025	-0.832	-0.832	10.609
P_{ACload}	1.800	12.500	12.500	4.200	4.200	15.300
P_{ACgen}	-5.000	-5.000	-5.000	-5.000	-5.000	-5.000

Based on the power flow values obtained at each case the losses at each conversion stage and the network losses were analysed. This is presented in Table 5-2.

Table 5-2: Loss analysis of SST

Detail	Losses (%)					
	Case 1	Case 2	Case 3	Case 4	Case 5	Case 6
AC line losses	6.54	6.54	6.54	3.85	3.85	2.91
DC line+ converter losses	8.5	10.95	11.27	11.50	10.71	9.87
AC-DC converter loss	4.85	2.15	3.10	4.03	4.03	2.15
DAB loss	4.76	1.96	2.25	5.12	4.76	2.06
DC-AC converter loss	6.28	4.31	4.21	6.28	6.28	4.49
Total SST losses	15.89	8.42	9.56	15.43	15.07	8.70

Based on the Table 5-2, the following observations were made:

- Despite the advantages served by the SST, its low efficiency is one of the major drawbacks. The proposed SST offers an average efficiency of 87%. The oil immersed LFTs offer a higher efficiency of around 99.5% [2]. The SST has multiple conversion stages and depending on the design and control of each converter, the losses at each conversion stage vary. High efficient SST converter design is not under the scope of this thesis.
- The SST losses decrease with increasing load levels. The proposed SST is designed with the capacity of 25 kVA. When the load level is higher and around 25

kVA the SST efficiency is higher. This is illustrated in Figure 5-4. This SST efficiency curve is directly related to the DAB efficiency curve as presented in [72]. The efficiency of LFT does not vary much with loading level. On the contrary, for SST it is observed that efficient operation of SST falls mostly in a limited range near to the rated load, below which the efficiency drops significantly. One of the reasons being, the operation of the SST outside the soft switching region.

- The SST efficiency also depends on load power factor as feeding inductive loads interrupts inductive current, which leads to increased switching losses [73]. Improved power factor leads to reduced losses. However, in this study all loads were assumed to be 0.85 power factor.

- A maximum loss of 11.27% can be observed for DC network losses, which include both converter losses and line losses. Compared to AC line losses, DC line losses contribute equally. Locating the ESD in the DC line stabilizes the DC line voltage compensating the voltage drop occurring due to line loss. Additionally, appropriate positioning of the DRER and ESD also affects the DC losses in the network. This was not analysed in this study hence considered as a suggestion for the future work.

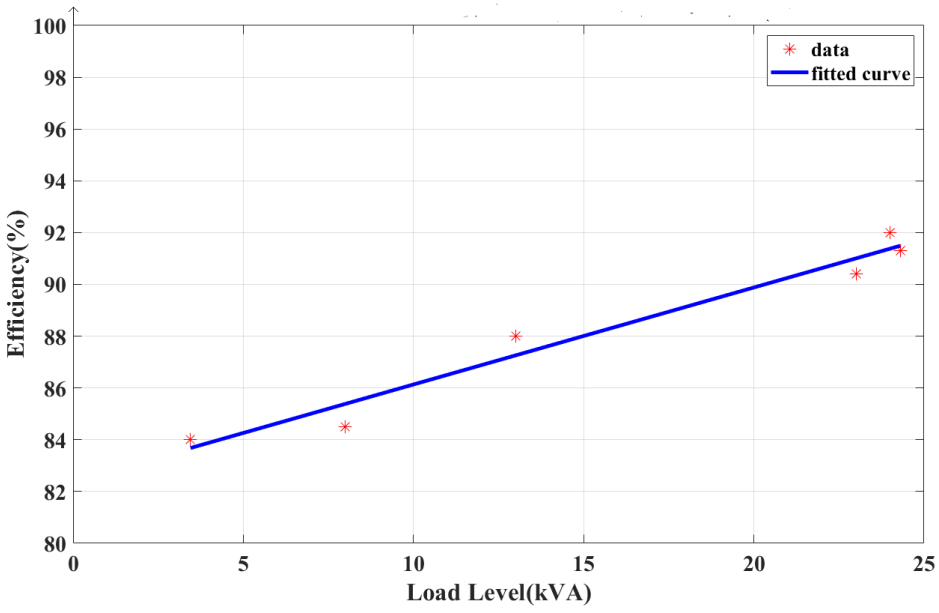


Figure 5-4: Load level Vs Efficiency of SST

It is worth comparing the DC distribution network loss in a hybrid system against the conventional AC distribution system. Since the majority of domestic and commercial loads employ DC power, the AC-DC power converters result in an additional loss of 4-15%. Additionally, applications using VFDs, like washing machines, ACs require an AC-DC converter and another converter to generate variable AC. This will further increase the conversion loss. Having a DC system eliminates the use of the AC-DC stage.

- With no DRER, DC line losses are comparatively low. Considering Case 1 and 6, which has no DRER, DC line losses are low. However, the DC loads are higher at Case 6, hence a significant reduction of losses cannot be observed.

5.2. Voltage variation along the feeder

The same power quality parameters discussed quantitatively in the existing network are analysed in the proposed system. For the better comparison, both results are presented in this section. Table 5.3 compares the voltage variation along the feeder at each pole of the existing system (shown in Figure 5-5 (a)) and the proposed system (shown in Figure 5-5 (b)) highlighting the observations. The pole IDs are given in Figure 4.2 in Section 4.1.

Table 5-3: Voltage variation along the AC feeder

Existing system	**Proposed SST based system**

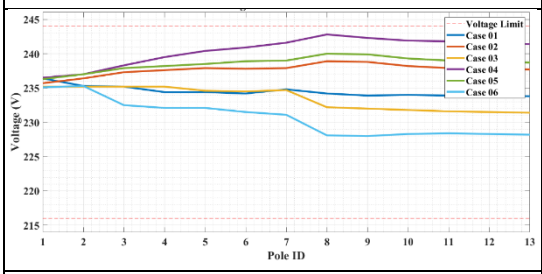
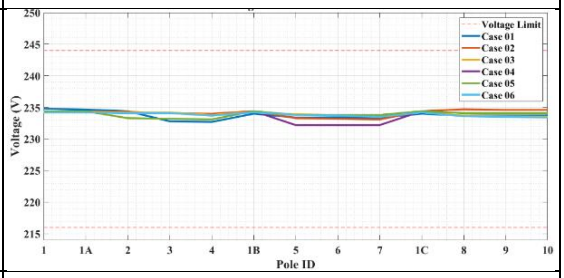

	

Figure 5-5 (a): Voltage variation along the AC feeder for the Existing system	Figure 5-5 (b): Voltage variation along the AC feeder for the Proposed system
• Does not exceed the regulated limits	• Does not exceed the regulated limits
• Maximum over voltage: + 5.2 %	• Maximum over voltage: +1.8 %
• Day time low loading condition increases the line voltage considerably	• Maintains nearly constant voltage at all the cases

Unlike in the existing system, the three microgrids in the proposed system have shorter feeder lengths. Hence, a significant voltage drop cannot be observed in all 6 cases. Since the solar PV are not connected to AC feeder, the AC voltage variation does not co-relate to the cases concerned. AC voltage is maintained same as the supply voltage from the transformer throughout the end of the feeder. At 1A, 1B, 1C poles the voltage has bit risen due the AC power generation by the 5 kW diesel generators.

Among many different DC bus structures, a radial bus structure was employed, due to its simplicity. The SST maintains the DC voltage at 700 V, and irrespective of the DC generation, at multiple nodes, DC bus voltage is maintained by the SST controller.

5.3. Voltage THD

Figure 5-6 (a) and (b) in Table 5.4 presents the VTHD levels along the AC feeder for the existing and proposed systems and Table 5.4 also summarises the observations related to VTHD in the existing system (presented in detail in Section 3.2.3), comparing with the observation of VTHD in the proposed system.

Table 5.4: VTHD of the AC feeder

Existing system	**Proposed SST based system**

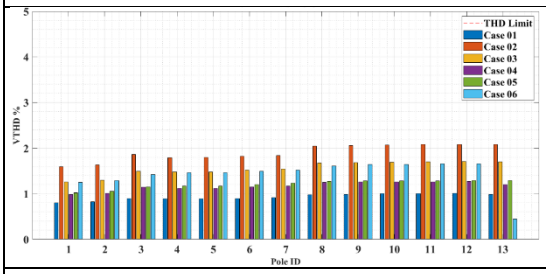
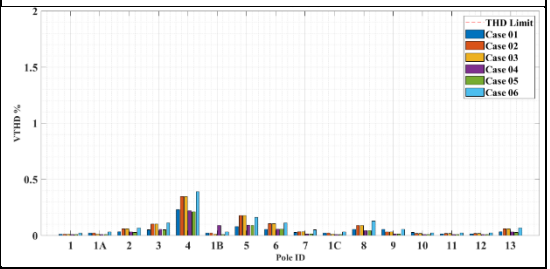

	

Figure 5-6 (a): VTHD of the AC feeder of the Existing system	Figure 5-6 (b): Figure 5-5: VTHD of the AC feeder of the Proposed system
• THD in accepted limits (< 8 %)	• THD in accepted limits (< 8 %)
• Maximum VTHD : 2 %	• Maximum VTHD : 0.4 %

In the proposed system, the AC feeder is not connected with solar PV. Hence, the only harmonic sources are the non-linear loads connected to the AC feeder. Also, a finite pattern cannot be observed on the VTHD and solar PV generation due to the fact that AC feeder has no connected solar PV. The total harmonic effect is thus reduced in all

the cases. At high loading (Case 2, 3 and 6), the non-linear load contribution increases and the harmonic distortion is higher than the other cases. Pole 4 is the highest loaded pole at all 6 cases. Therefore, VTHD of Pole 4 is high at all 6 cases. At pole 1: the transformer output, the VTHD is the minimum as the supply voltage waveform is undistorted by the utility grid. At the poles 1A, 1B and 1C where the SST AC output port is connected, slightly higher THD is observed because of the inverter output.

5.4. TDD

Figure 5-7 (a) and (b) in Table 5.5 presents the TDD levels along the AC feeder for the existing and proposed systems and Table 5.5 also summarises the observations related to VTHD in the existing system (presented in detail in Section 3.2.4), comparing with the observation of VTHD in the proposed system.

Table 5.5: TDD of the AC feeder

Existing system	**Proposed SST based system**

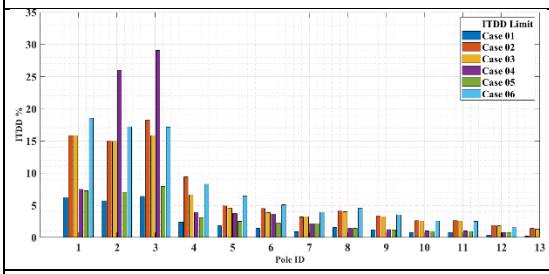
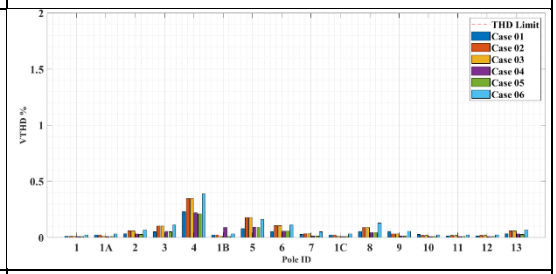

	

Figure 5-7 (a): TDD of the AC feeder of the Existing system	Figure 5-7 (b): Figure 5-6: TDD of the AC feeder of the Proposed system
• Up to bus 7, all buses including the transformer secondary had exceeded the stator limit of current harmonics level of 5 %.	• TDD in accepted limits in the AC feeder
• At low irradiances, ITHD rises	• Maximum TDD : 0.4 %

TDD values were calculated based on the maximum current at each SST. When considering SST 1, which has three poles 2, 3, 4, the maximum current flows at pole 2. Hence, the current at pole 2 was selected as the base current to calculate the TDD at

pole 2, 3, and 4. Similarly TDD was calculated for other SSTs. A correlation does not exist between the solar penetration level and the TDD similar to the VTHD. According to the general tendency of the harmonic current flow, the distortion should be higher towards the SST [2]. This can be observed from Figure 5-7 (b), highest TDD levels recorded in pole 2, 5 and 8. Since the only harmonic source is the non-linear loads at the AC feeder, an overall maximum reduction of 29.5% can be observed for TDD levels.

5.5. DC Injection

The following conclusions were derived from Section 3.2.5 based on the DC injection of the existing system.

- Exceeds 1% DC injection (measured based on the current across the feeder at that point of measurement)
- At the transformer secondary a considerably high percentage of DC current of 0.6 A was observed

However, the DC injection level of the AC feeder of the proposed system is 0 since there are no any DC injection sources. The isolated DC bus also prevents DC injection towards the upstream feeder. However, at the transformer secondary terminal, (Pole 1) a DC injection current of 0.04 A was observed. This is shown in Figure 5-8.

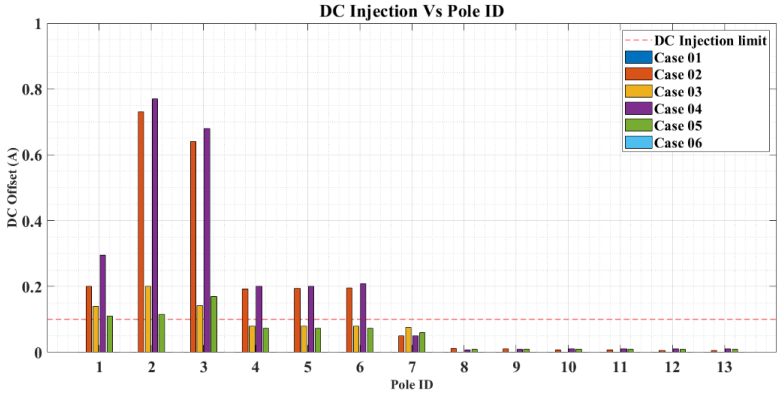


Figure 5-8: DC Injection along the AC feeder of the existing system

CHAPTER VI

6. CONCLUSION AND FUTURE WORK

This chapter presents the main contributions of the study and the conclusion of this research. In addition, it proposes the directions for future research in the SST microgrid design and control.

6.1. Summary

The main objective of this thesis was to study the technical issues due to high penetration of rooftop solar PV with grid tie inverters and design a grid connected SST based hybrid microgrid to mitigate the issues identified. A 40% solar PV penetrated distribution feeder (based on the transformer capacity) was selected as the case study. Based on the smart meter data collected (by the local DSO: LECO) over one-month time, load data was obtained. MATLAB/Simulink model was developed and the power quality parameters such as voltage variation, VTHD, TDD and DC injection were analysed considering 6 different cases.

The same AC distribution feeder was re-designed to accommodate three zonal AC/DC hybrid microgrids. The full feeder was divided into three zones and each zone had a different loading level and a generation based on the field data. The SST was located at the PCC of the microgrid and the main-grid. Design of the SST to accommodate the hybrid microgrid and the control of it were the main objectives. The AC-DC converter, DC-DC converter and the DC-AC inverter were designed and three controllers for each conversion stage were developed based on the control objectives at each stage. The DCMG consisted of the ESD, DC loads and solar PV. The ACMG consisted of AC loads (linear and non-linear) and an AC generator. Each system was separately tested under different criteria and integrated to function the full feeder with three zonal microgrids interfaced with SSTs.

The developed system was finally tested for its power quality parameters rectified in the existing system. Having the solar PV are connected to the DC bus, the harmonic content in the feeder was reduced drastically. The DC-DC isolation of the SST does

not allow the DC injection towards the upstream network. Without distributed generation along the AC feeder, the voltage rise issue was also mitigated significantly.

Even though the test system was a traditional distribution feeder, the proposed model can be used within a smart city. A localized SST based microgrid will be powering a limited geographical region and several such microgrids can be sued to power a smart city. Community microgrids have already been established and therefore the proposed architecture can be integrated for powering the smart cities.

6.2. Conclusion

The future power distribution industry is moving towards a distributed network than a centralized system. The drastic growth of distributed generation from the customers should be expected in the near future. However, the DSO should maintain the power quality of the national grid. Improving the hosting capacity of solar PV in the distribution network has thus become a hot topic in the power systems industry.

From this study, it was identified that the voltage rise, THD, TDD and DC injection into the upstream network as the major technical issues due to increasing distributed solar PV penetration. The proposed SST based hybrid microgrid systems provide significant improvements over the conventional distribution network. Maximum over voltage was reduced by 3.4%, VTHD reduced by 1.5 %, TDD reduced by 29.5 %, and the DC injection was eliminated by the SST design itself. In addition, the active power flow management of the microgrid was handled by the SST, based on the phase shift of the power flow. The SST controllers were responsible in maintaining the AC, DC feeder voltages.

The isolation of the load harmonics (contribution from PV inverters and nonlinear loads) by the DC-DC isolation is the biggest advantage to the utility power quality. The other advantage gained from the proposed system is that the ability to connect DC loads, distributed generation and ESD directly to the DC bus, reducing the conversion losses significantly. The proposal of zonal microgrids with shorter feeder lengths eliminate the requirement to place ESDs along the DC distribution feeder. These functionalities ultimately improve the overall power quality of the system. However, it cannot be denied that the large number of elements that integrate the SST (semi-

conductors switches, HFT, controllers, filters) will have an impact on its reliability. In addition, the low efficiency of the SST is another challenge identified from this study. The proposed SST resulted in an efficiency of 87%, which is lower than a LFT (with efficiencies around 99%). Despite the low efficiency and low reliability, the benefits offered by SST technology thus cannot be under-rated. Following the future technological advancements in the semiconductors, it is expected that the SST will improve its efficiency and reliability, thus closing the gap with respect to the LFT.

The proposed SST based distribution hierarchy, can provide both the consumer and the utility a superior controllability and improvement of power quality over the existing passive LFT based distribution system. The overall hosting capacity of the proposed system has thus been improved in the proposed network allowing more penetration of rooftop solar PV without violating the network standards.

Integrating more renewables to the grid and improving power quality are ultimately paving the way for more sustainable and reliable networks. Localized smart cities are being researched based on microgrid concept [78]. The proposed SST based microgrid architecture with multiple microgrids facilitate the concept of smart cities. Ultimately cities with improved power quality, resilience and high penetration of solar PV will be created as local networks rather than centralized and synchronized traditional power networks,

6.3. Future work

- Selection of the optimum operative high frequency for the SST is a major design factor. Increased frequencies increase the system losses. Reduced frequencies increase the overall size of the transformer. Therefore, the optimizing of the frequency and the size of the transformer is a major concern. However, in this design 20 kHz was selected as the switching frequency based on the trade-off between volume/weight and efficiency [60]. The fact that many typical IGBT applications employ 20 kHz is also another reason to choose 20 kHz. However, a proper optimization study for the selection of the frequency will guarantee better

SST performance.

- The hosting capacity calculation based on multiple power quality parameters has not been done in the study. Any hosting capacity study requires a performance index, a statutory limit; and a method to calculate the value of the performance index as a function of the amount of new production or consumption [79]. Many studies have been done looking at the hosting capacity based on factors like over-voltage, under-voltage and overcurrent. However, acceptable calculation models for evaluating the hosting capacities including harmonics as a factor, remains missing and further work is needed in this area [79]. The calculation of hosting capacity based on multiple power quality parameters, which include voltage, harmonics and DC offset is suggested.

- The LFT in this proposal at the interface of the SST and the grid serves MV (11 kV) to LV (400 V) conversion. If this LFT is replaced with one SST, the use of zonal microgrids will be unnecessary. Single SST with higher capacity could have served the whole distribution feeder if it was designed in modular multi-level topology. Designing an MMC based microgrid to exploit these advantages is suggested as a future work. However, zonal microgrids inherits higher system reliability with required system stability and power quality compared to having a single MMC microgrid with a complex control scheme.

- The main objective of this study was to mitigate the impacts caused due to high solar penetration. The SST design by itself, with its distributed controllers have achieved this objective. Fault current mitigation, power factor improvement, reactive power compensation can be additionally incorporated into the same design for improved performance.

- The proposed SST model, in this study absorbs only active power from its MV terminal and regulates constant LV voltage. The required reactive power to the ACMG is supplied by the AC link capacitance. The control architecture can be designed as required flexibility to incorporate other features of the SST. For

example, SST can inject reactive power into the MV grid if some voltage support is required, and maintaining the terminal voltages at the LV side at statutory limits. These two potential strategies (i.e., control of LV-side voltage and MV-side reactive power) are proposed as future work.

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APPENDICES

Appendix A: Matlab code for the MPT controller using P & O algorithm

```
function Duty  = PandO(Param, Enabled, PV_V, PV_I)

% Duty =  Boost converter duty cycle (0-1)

Dinitial = 0.62;  %Initial value for D output
Dmax = 0.8;   %Maximum value of D
Dmin = 0.2;   %Minimum value of D
Ddelta = 2e-4; %Value used to vary D

persistent PV_Vold PV_Pold Dold;

dataType = 'double';

% Initializing from 0
if isempty(PV_Vold)
   PV_Pold=0;
   PV_Vold=0;
   Dold=Dinitial;
End

% PV_V = Terminal voltage of the PV (V)
% PV_I = Current of the PV (A)
P= PV_V*PV_I;

% Increasing Duty= decreasing reference voltage
dV= PV_V - PV_Vold;
dP= PV_P - PV_Pold;

if dP ~= 0 & Enabled ~=0
%Enabled Input =1 (enable the MPPT control)
   if dP < 0
      if dV < 0
         Duty = Dold - Ddelta;   % Decreasing D when PV-V < PV-Vold  and
PV-P < PV-Pold
      else
         Duty = Dold + Ddelta;  % Increasing D when PV-V > PV-Vold and
PV-P < PV-Pold

      end
   else
      if dV < 0
```

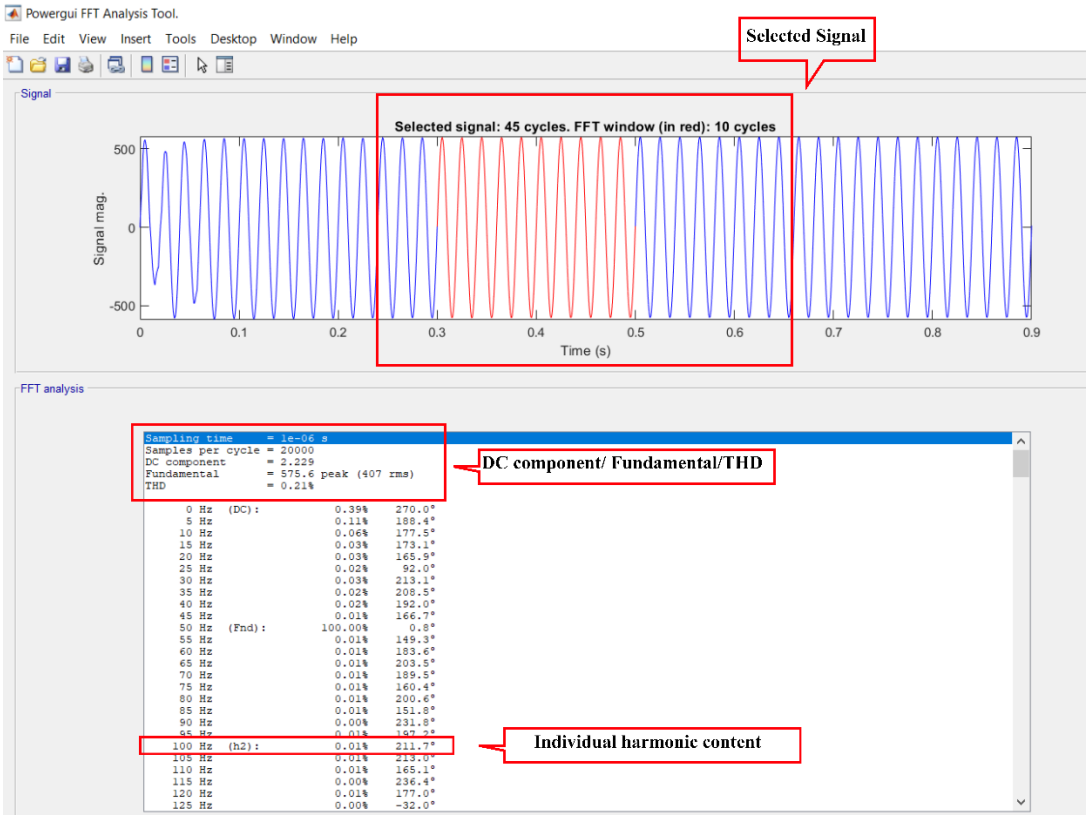
```
            Duty = Dold + Ddelta;
        else
            Duty = Dold - Ddelta;
        end
    end
else Duty=Dold;
end

if Duty >= Dmax | Duty<= Dmin
    Duty=Dold;
end

PV_Vold=PV_V;
Dold=Duty;
PV_Pold=PV_P;
```

Appendix B: Calculation of the THD from FFT analyser in SIMULINK

Once the voltage or current signal data is output to a scope and save the selected data into the workspace, the FFT analyser loads the signal and calculate the harmonic content in the signal. This is shown in Figure B-1.



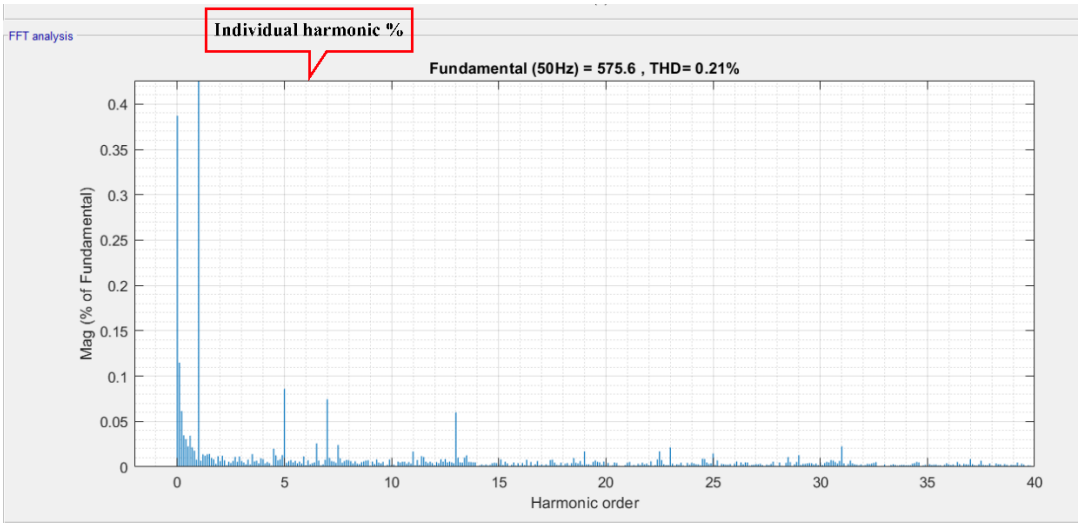


Figure B-1: FFT analyser window of SIMULINK

Appendix C: Simulink models

Figure C-1: Full feeder with 3 SSTs modelled in simulink

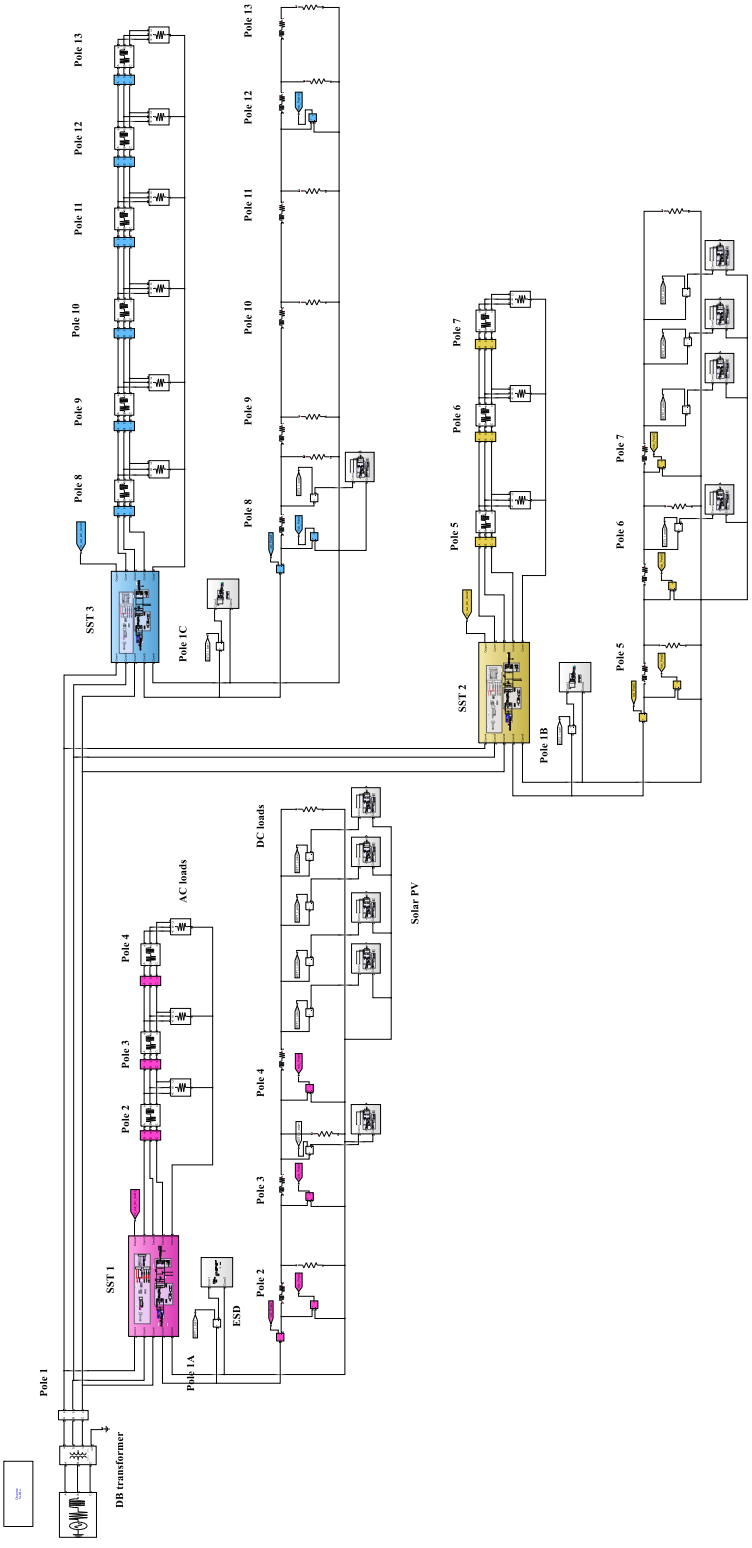
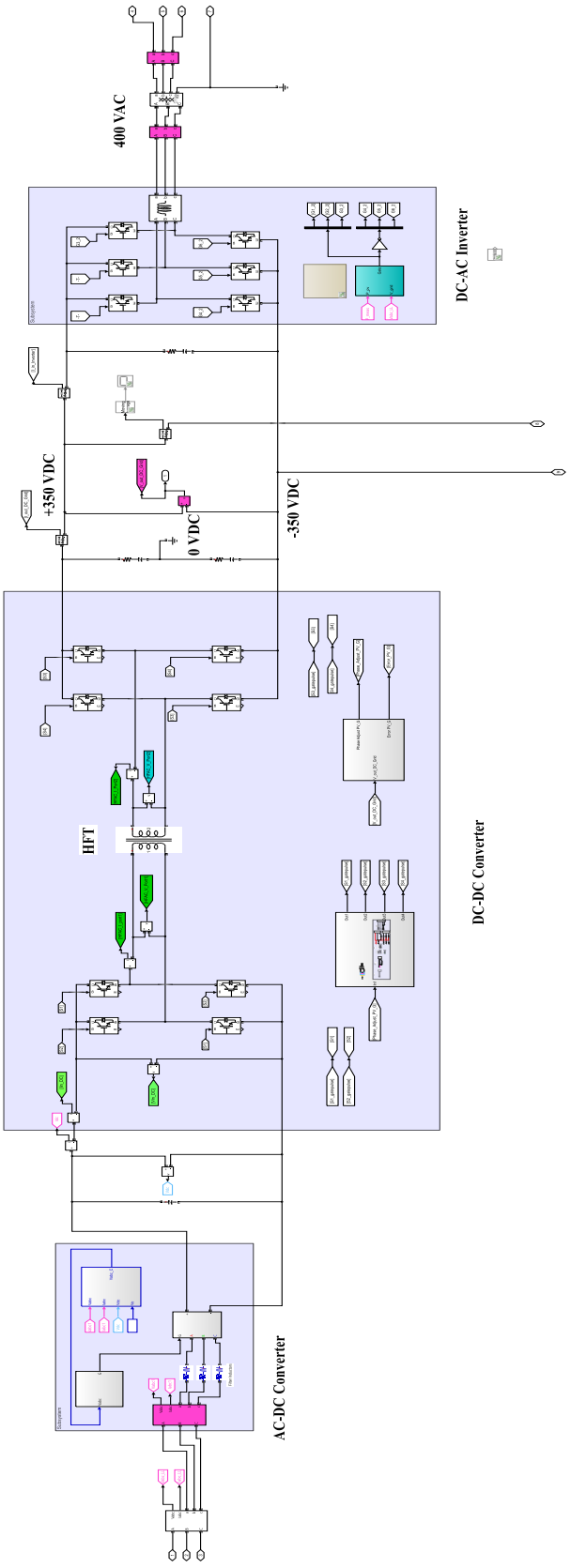


Figure C-2: SST 1 Model with three converter stages



Appendix D: Proposed operating modes of the ESD

An ESD management for the proposed microgrid system was not implemented. However, possible power management modes for the proposed system are presented in Figure C-2. The developed system was designed only to operate in the grid connected Battery charging modes 1- 4. Power flow and converter operating status also depends on ESD SoC levels. In the grid connected mode, if the SoC is lesser than SoC_{max} (0.9), and if the generation is higher than the load, the battery charges from constant current charging (Mode 1). If the generation is less than the load, battery is charging from the grid, under the condition $SoC < SoC_{max}$ (Mode 3). Since the system is designed only to operate under charging mode, if the SoC is higher than SoC_{max}, the battery is in idle mode which represent mode 2 and 4.

The suggested criteria for the ESD to operate in the islanded mode is presented in detail in Table D-1. In the grid connected mode, DC bus voltage is regulated by the grid. In the islanded mode, ESD should maintain the voltage of the system. Therefore, the battery should be charged under constant voltage to maintain the DC bus voltage at 700 V. Maximum charging current is limited to 20 A.

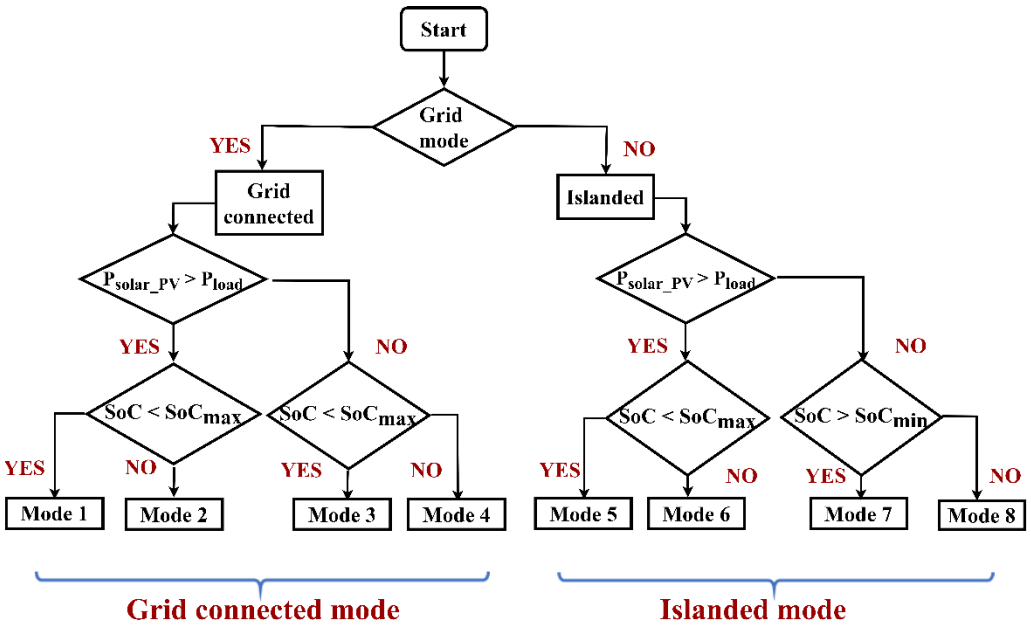


Figure D-1: ESD Management algorithm for the proposed system

Table D-1: ESD Operating modes in detail

Grid Connected operation	Mode 1 $P_{solar\_PV} > P_{load}$ $SoC < SoC_{max}$ • Battery charges in constant current mode (I_{bat}^{ref}=10A) • DC bus Primary control: SST ($V_{SST\_DC}^{ref}$ =700V)	Mode 2 $P_{solar\_PV} > P_{load}$ $SoC = SoC_{max}$ • Battery operates at idling mode (Ibat=0) • DC bus Primary control: SST (VSST_DCref =700V)
	Mode 3 $P_{solar\_PV} < P_{load}$ $SoC < SoC_{max}$ • Battery charges in constant current mode (Ibatref=10A) • DC bus Primary control: SST (VSSTref =700V)	Mode 4 $P_{solar\_PV} < P_{load}$ $SoC = SoC_{max}$ • Battery operates at idling mode (Ibat=0) • DC bus Primary control: SST(VSSTref =700V)

Islanded operation	Mode 5 $P_{solar\_PV} > P_{load}$ $SoC < SoC_{max}$ • Battery charges in constant voltage mode (Vbat_DCref =700V) • Battery storage takes over DC bus voltage control • Maximum charging current is limited at 20A • DC bus Primary control: Battery storage system	Mode 6 $P_{solar\_PV} > P_{load}$ $SoC = SoC_{max}$ • Generation curtailment; Solar PV are required to operate in voltage control mode (Vboostref=700V) or immediately shutdown the whole network. • Battery operates at idling mode (Ibat=0) • DC bus Primary control: generation curtailment (Solar PV)
	Mode 7 $P_{solar\_PV} < P_{load}$ $SoC_{min} < SoC$ • Battery discharges in constant voltage mode (Vbat_DCref =700V) • Battery storage takes over DC bus voltage control • Maximum charging current is limited at 20A • DC bus Primary control: Battery storage system.	Mode 8 $P_{solar\_PV} < P_{load}$ $SoC = SoC_{min}$ • Load shedding; loads are required to be shed to maintain network stability or immediately shutdown the whole network. • Battery operates at idling mode (Ibat=0) • DC bus Primary control: load shedding